CR-184034

MCR-90-536
Contract No. NAS8-36583

Final
Report

July 1990

Space Station Common Module Network Topology and Hardware Development

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SPACE STATION
COMMON MODULE NETWORK TOPOLOGY
AND HARDWARE DEVELOPMENT

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This report was prepared by Martin Marietta Denver Astronautics Group for the National Aeronautics and Space Administration, George C. Marshall Space Flight Center (NASA/MSFC), in response to contract NAS8-36583. This Final Report is submitted to the Electrical Power Branch at NASA/MSFC as specified in the contract data requirements list.

A	Amps
A/D	Analog to Digital
AC	Alternating Current
COR	Contracting Office Representative
DC	Direct Current
EPS	Electrical Power System
GC	Generic Controller
GFP	Ground Fault Protection
GND	Ground
HZ	Hertz (Cycles/Second)
I^2t	Product of Current Squared and Time
LLP	Lowest Level Processor
MMAG	Martin Marietta Astronautics Group
MSFC	George C. Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
PDCU	Power Distribution Control Unit
RBI	Remote Bus Isolator
RCCB	Remote Controlled Circuit Breaker
RPC	Remote Power Controller
SIC	Switchgear Interface Controller
SPST	Single Pole Single Throw
SSM/PMAD	Space Station Module Power Management and Distribution
SOW	Statement of Work
V	Volts
W	Watts

1.0 INTRODUCTION

This document reports on Contract NAS8-36583 and is in response to the work which was performed in developing and delivering hardware for the Space Station Common Module Network Topology and Hardware Development contract. This work was performed by Martin Marietta Corporation, Denver Astronautics Group for the National Aeronautics and Space Administration, George C. Marshall Space Flight Center, in support of the Electrical Power Branches' development of an automated power distribution system test bed. The NASA Contracting Officer's technical representative for the contract is Ms. Cindy Thomason. Martin Marietta is reporting on Tasks I, II, III, and IV of the contract.

Task I	Common Module Power Management and Distribution System Preliminary Definition
Task II	Hardware Selection
Task III	Hardware Advanced Development and Verification Test
Task IV	Common Module Power Management and Distribution Breadboard Testing

2.0 TASK I

Space Station Common Module Power Management and Distribution System Preliminary Definition

The purpose of Task I was to develop conceptual Space Station Common Module Power Management and Distribution (SSM/PMAD) network layouts, develop detailed network evaluations, and to identify individual pieces of hardware to be developed for the SSM/PMAD test bed.

2.1 SSM/PMAD Requirements Definition

The requirements in the Statement of Work (SOW), the Martin Marietta Astronautics Group (MMAG) SSM/PMAD requirements, the former revision of the Space Station Reference Configuration Description, and the space station system efforts as defined in the C2, C3 and C4 specifications were analyzed and used to develop a set of baseline SSM/PMAD requirements. These requirements were reviewed with the Marshall Space Flight Center (MSFC) Contracting Officer Representative (COR) early in the program and are listed in Table 2.1-1.

2.2 Loads Analysis

A space station loads data base was developed from a previously existing space station loads analysis data base as reflected in Table 2.2-1. This provided a point of departure to develop switchgear current carrying requirements.

2.3 Conceptual Network Layouts

Conceptual network layouts were developed based on functional, configuration and energy storage candidate networks as supplied by MSFC. Several ground rules were established which were taken into account in developing the conceptual layouts:

1. Redundancy - a) Each load will have a minimum of two paths back to the primary power source; b) redundancy will be implemented to such a degree as to identify all

Table 2.1-1 CM/PMAD Requirements

	Requirement	Source Document/ Paragraph #
1.	The CM EPS shall convert and condition primary distribution system power to the types best suited for distribution. Within the CM, the power shall be distributed, monitored, circuit protected and controlled. Power networks shall be provided for all avionics.	SS-SRD-100/ 2.2.3.1
2.	Accept power from redundant utility buses. Loss of one functional path will not result in the loss of the alternate redundant path.	C-4/2.1.10.4
3.	Diverse routing of redundant wiring and equipment shall be implemented.	C-4/2.2.3.h
4.	The design shall preclude a single open circuit causing loss of the bus.	C-4/2.2.3.h
5.	The design shall provide verification of redundancy without ORU removal.	C-4/ 2.1.10.2.a
6.	The EPS shall provide both redundancy status and management.	C-4/ 2.1.10.2.b
7.	Redundant accommodations for complete command and control shall be provided in separate locations.	SS-SRD-100/ 2.1.11.4.b
8.	A means of selecting/deselecting prime power buses and loads shall be provided.	C-4/2.2.3.f
9.	Power sources and distribution shall be protected against overloads and faults.	C-4/2.2.3.e
10.	All wiring shall be protected at the source or be current limited.	C-4/2.2.3.h
11.	All circuit protection devices shall be resettable or replaceable.	C-4/2.2.3.h
12.	Ground fault protection shall be provided on circuits that are accessible.	C-4/ 2.1.11.2.k
13.	The design shall preclude failure propagation.	C-4/2.1.10.3
14.	All equipment shall be easily removed and replaced at the ORU level.	C-3/3.2.a
15.	The system shall be capable of undergoing maintenance without interruption of critical services or other SSPE operations.	C-4/2.1.9.d
16.	Maintenance shall not cause hazardous or destructive conditions.	C-4/2.1.9.g

Table 2.1-1 CM/PMA Requirements (Concl).

	Requirement	Source Document/ Paragraph #
17.	Subsystem design shall accommodate ORU replacement at any time.	C-4/2.1.9.i
18.	Independent subsystems shall be developed to facilitate operations/ maintenance.	C-3/3.2.j
19.	The ORU shall provide monitoring, checkout and fault detection and isolation to the ORU without removing the ORU.	C-4/2.1.9.c
20.	The EPS shall support hardware communality to the maximum extent practical to facilitate system growth.	C-4/2.1.5
21.	The design shall accommodate new technology as appropriate to optimize benefits to the program.	C-4/2.1.6
22.	The subsystem shall have the capability to progressively modified or upgraded on orbit to accommodate evolving technologies.	C-3/2.1.a
23.	Provide power to safe haven.	C-4/2.2.3.i
24.	The design shall accept probable primary input power types: a) High frequency 1 ø AC; b) Low frequency (<1 kHz) single or multiphase AC at > 150 AC (rms); c) ≥ 150 Vdc.	Task I.a/ (RFP)
25.	The design shall have the capability for distributing 25 kW internal and 25 kW external. The system shall be redundant.	SS-SRD-100/ 2.2.3.2
26.	The design shall provide the capability of distributing utility power.	C-4/2.2.3.c
27.	Safety or mission critical functions shall be fail/op fail safe restorable.	C-3/2.2.c
28.	The crew shall not be exposed to high voltage power leads.	C-4/2.1.11.k
29.	The design shall employ an electrical single point ground.	C-4/2.2.3.g
30.	Manual overrides and inhibits shall be provided for automated functions.	C-3/3.3.b
31.	The EPS network configuration shall be transparent to the energy conversion and storage technologies selected.	Task I.e/ (RFP)
32.	Hardware design shall be electromagnetic compatible.	Derived
33.	Control systems (i.e., switchgear, sensors) shall provide outputs which may be integrated with the automation control system.	Derived from C-3/3.3.a
34.	The CM/PMAD shall be capable of surviving decompression.	

Table 2.2-1 Space Station Loads Data Base

SUBASSY	NOMINAL	DUTYCYCL	MIL	HB1	HB2	LOG	LSL
C02 Removal	157.000	1.00000	1	1	1	-0-	1
C02 Reduction	294.000	1.00000	1	1	1	-0-	1
02 Generation	1597.00	1.00000	1	1	1	-0-	1
Urine Hygiene Processing	40.0000	-0-	-0-	1	1	-0-	-0-
Urine Hygiene Processing	550.000	1.00000	-0-	1	1	-0-	-0-
Potable Water Processing	550.000	1.00000	1	1	-0-	-0-	-0-
Potable Water Processing	20.0000	1.00000	1	1	1	-0-	1
H20 Storage & Distribution	3.00000	-0-	-0-	1	1	-0-	-0-
Trash Coll. & Processing	15.0000	1.00000	-0-	1	-0-	1	-0-
Propellant Tanks	12.0000	0.50000	-0-	-0-	-0-	-0-	-0-
Pressure Transducers	0.60000	1.00000	-0-	-0-	-0-	-0-	-0-
Pressure Transducers	0.60000	1.00000	-0-	-0-	-0-	-0-	-0-
Propellant Tanks	12.0000	0.50000	-0-	-0-	-0-	3	-0-
Pressure Transducers	0.60000	1.00000	-0-	-0-	-0-	7	0
Propellant Tanks	12.0000	0.50000	-0-	-0-	-0-	-0-	-0-
Pressure Transducers	0.60000	1.00000	-0-	-0-	-0-	7	-0-
Battery/Charger-Log	35.0000	1.00000	-0-	-0-	-0-	2	-0-
-0-	80.0000	1.00000	-0-	-0-	-0-	-0-	-0-
Sputtering Deposition Unit	1700.00	0.08000	1	-0-	-0-	-0-	-0-
Mass Measurement System	100.000	0.16000	1	-0-	-0-	-0-	-0-
Metallographic Microscope	200.000	0.16000	1	-0-	-0-	-0-	-0-
X-ray Topography Unit	1500.00	0.16000	1	-0-	-0-	-0-	-0-
UV/VIS/NIR Spectrometer	250.000	0.16000	1	-0-	-0-	-0-	-0-
Optical Microscope	50.0000	0.25000	1	-0-	-0-	-0-	-0-
Low Speed Centrifuge	250.000	0.33000	1	-0-	-0-	-0-	-0-
Hall Probe	500.000	0.16000	1	-0-	-0-	-0-	-0-
Auto. Cut & Polishing Unit	750.000	0.42000	1	-0-	-0-	-0-	-0-
Hi-Perf. Liq. Chromatograph	2500.00	0.16000	1	-0-	-0-	-0-	-0-
Scanning Electron Microsc.	1500.00	0.25000	1	-0-	-0-	-0-	-0-
Fourier Trnsfrm IR Spect.	750.000	0.25000	1	-0-	-0-	-0-	-0-
Gas Chromgph-Mass Spectro.	4000.00	0.16000	1	-0-	-0-	-0-	-0-
Elec Conductivity Probe	150.000	0.04000	1	-0-	-0-	-0-	-0-
Battery Charger	20.0000	0.50000	1	-0-	-0-	-0-	-0-
Liq./Solid Seperation Sys.	200.000	0.08000	1	-0-	-0-	-0-	-0-
Fluids Glovebox	200.000	0.25000	1	-0-	-0-	-0-	-0-
Master Computer	1000.00	1.00000	1	-0-	-0-	-0-	-0-
3-Axis Rec. Accelerometer	50.0000	1.00000	1	-0-	-0-	-0-	-0-
Freeze Drier	500.000	0.08000	1	-0-	-0-	-0-	-0-
Video Facilities	100.000	0.33000	1	-0-	-0-	-0-	-0-
Waster Disposal System	750.000	0.50000	1	-0-	-0-	-0-	-0-
-0-	150.000	0.01000	2	2	2	2	2
-0-	300.000	0.37500	-0-	1	-0-	-0-	-0-
-0-	150.000	0.04160	1	1	1	1	1
Annunciator Unit	5.00000	0.01000	2	1	1	-0-	1
Remote Annunciator	1.00000	0.01000	1	3	3	4	3
Mag Disk (600 MBIT)	10.0000	0.50000	3	2	2	-0-	3
Mag Tape (1000 GBIT)	10.0000	0.50000	1	1	1	-0-	2
Bus Interface Units	5.00000	1.00000	55	14	14	12	16
Gateway Interface Unit	10.0000	1.00000	3	2	2	2	2

Table 2.2-1 Space Station Loads Data Base (Cont'd)

SUBASSY	NOMINAL	DUTYCYCL	MIL	HB1	HB2	LOG	LSL
Subsystem Controller	30.0000	1.00000	23	14	14	12	16
Dedicated Controller	50.0000	1.00000	36	54	28	36	24
Circulation Fan	650.000	1.00000	1	1	1	1	1
Cabin Fan Package	730.000	1.00000	2	2	2	2	2
Temp Controller	31.0000	1.00000	2	2	2	2	2
Bulk Storage Freezer	495.000	0.50000	-0-	-0-	-0-	1	-0-
Freezer	495.000	0.50000	-0-	1	-0-	1	-0-
02/N2 Pressure Controller	30.0000	1.00000	1	1	1	1	1
Vent & Relief	17.0000	0.01000	1	1	1	1	1
Primary Power Dist. Assy.	20.0000	1.00000	2	2	2	-0-	2
Secondary Distrib. Assy.	20.0000	1.00000	2	2	2	2	2
Subsystem Load Center	20.0000	1.00000	3	3	3	2	3
Exterior Light Controller	10.0000	1.00000	4	4	4	4	4
Int. Light Controller	220.000	0.67000	2	2	2	2	2
Emergency Lighting	20.0000	1.00000	2	2	2	2	2
-0-	8.40000	0.20000	2	2	2	2	2
-0-	20.0000	1.00000	4	2	2	2	2
-0-	42.0000	1.00000	1	1	1	1	1
-0-	35.0000	0.20000	1	4	4	1	2
Pump Package	276.000	1.00000	2	2	2	1	2
Control Valves	69.0000	1.00000	19	14	14	9	14
Pressure Sensor	0.84000	1.00000	4	2	2	1	2
Flow Meter	0.84000	1.00000	8	6	6	4	6
Pump Package	371.000	1.00000	2	2	2	-0-	2
Control Valve	92.0000	1.00000	1	1	1	-0-	1
Pressure Sensors	0.84000	1.00000	2	2	2	-0-	2
Flow Meter	0.84000	1.00000	4	4	4	-0-	4
Ext. Power Condition Assy	30.0000	1.00000	-0-	-0-	-0-	-0-	-0-
Ext. DC Power Conditioning	30.0000	1.00000	-0-	-0-	-0-	-0-	-0-
Valve Drive Amp Assy	45.0000	1.00000	-0-	-0-	-0-	-0-	-0-
Power Condition Assy	20.0000	1.00000	4	2	2	-0-	2
Particulate Glovebox	250.000	0.75000	1	-0-	-0-	-0-	-0-
Data Recording Unit	100.000	1.00000	1	-0-	-0-	-0-	-0-
H20 Detonizer/Depyrogeniz	3000.00	0.50000	1	-0-	-0-	-0-	-0-
UV Sterilization Oven	150.000	0.08000	1	-0-	-0-	-0-	-0-
Port. UV Sterilization Ut	100.000	0.08000	1	-0-	-0-	-0-	-0-
Optical Pyrometer	20.0000	0.08000	1	-0-	-0-	-0-	-0-
Dig. Reading Oscilloscope	100.000	0.50000	1	-0-	-0-	-0-	-0-
Stereo Macroscope	20.0000	0.08000	1	-0-	-0-	-0-	-0-
Freezer	500.000	1.00000	1	-0-	-0-	-0-	-0-
Refrigerator	300.000	1.00000	1	-0-	-0-	-0-	-0-
Latex Reactor System	100.000	1.00000	1	-0-	-0-	-0-	-0-
Protein Crystal Growth FC	500.000	0.75000	1	-0-	-0-	-0-	-0-
Direct Solidification Fur	15000.0	0.83000	1	-0-	-0-	-0-	-0-
Droplet Combustion Facil.	500.000	0.16000	1	-0-	-0-	-0-	-0-
Controlled Atmosphere Fur	3500.00	0.50000	1	-0-	-0-	-0-	-0-
Electrophoresis Facility	3000.00	0.75000	1	-0-	-0-	-0-	-0-
Vapor Crystal Growth Fur	2000.00	0.83000	1	-0-	-0-	-0-	-0-
Acoustic Contrless Pr Fac	5000.00	0.50000	1	-0-	-0-	-0-	-0-

Table 2.2-1 Space Station Loads Data Base (Concl)

SUBASSY	NOMINAL	DUTYCYCL	MIL	HB1	HB2	LOG	LSL
Glass Fiber Pulling Fac	2000.00	0.16000	1	-0-	-0-	-0-	-0-
Process Air Dist. Bus.	117.600	1.00000	1	1	1	1	1
Contam Cntrl & Monitor Ct	126.000	1.00000	1	1	1	-0-	1
Atmos & Cont Monitor	26.0000	1.00000	1	1	1	1	1
Atmos & Cont Monitor	165.000	1.00000	1	1	1	1	1

switchgear, sensors, or other hardware needed for the Space Station Common Module PMAD.

2. Commonality - A standard control and monitor interface concept will be selected ensure maximum system flexibility.

3. Current Monitors - Switchgear will contain the necessary current monitors to perform current limiting and fault protection. Precision current monitors required for load management will be separate devices.

4. Ground Fault Protection (GFP) - Remote power controllers located in the load control centers will contain built-in ground fault protection. This feature will not be provided in the primary and secondary distribution assemblies. The purpose of GFP is to protect personnel from shock hazards and is necessary only at the lowest level of power distribution.*

   * Note: The 20 kHz RPCs developed for the NASA-MSFC breadboard incorporate this feature. However, the breadboard DC RPCs do not contain ground fault detectors due to the grounding configuration which was implemented into the breadboard system (the RPC switches only switch the "hot" side of the power and is therefore unable to perform ground fault detection).

During Task I, Martin Marietta developed four breadboard network schematics which reflected the three main power distribution options which were relevant at the time (200 Vac single-

phase 20 kHz, 115 Vac three-phase 400 Hz and 150 Vdc). The baseline at this time was the 115 Vac, three-phase, 400 Hz option.

Each of these power distribution options were developed into breadboard network schematics as shown in Figures 2.3-1 through 2.3-4. Each breadboard network contained primary and redundant power buses feeding five racks. Rack 1 was the primary distribution center and contained "bulk" converters for the applicable options (Options 2, 3 and 4). Each option contained a 115 V, 400 Hz system distributor (rack 2) and some post-conditioning at the rack user level. Option 1 (Figure 2.3-1) was a 115 Vac, 400 Hz system with post-conditioning to 115 Vac, 60 Hz, 150 Vdc, and/or 28 Vdc (rack 5 level). Option 2 (Figure 2.3-2) was a 115 Vac, 400 Hz power source with bulk conversion to 150 Vdc for distribution to user racks 2, 4 and 5. Post conditioning is shown in rack 5 to 115 Vac, 60 Hz and/or 28 Vdc. Option 3 (Figure 2.3-3) utilized a 150 Vdc power source with bulk conditioning to 115 Vdc, 400 Hz for use in the secondary distributor (rack 2). Post-conditioning is shown in rack 5 to 115 Vac, 60 Hz, 115 Vac 400 Hz and/or 28 Vdc. Option 4 (Figure 2.3-4) utilized a 200 Vac 20 kHz power source with bulk conditioning to 150 Vdc for distribution to racks 2, 3 and 5. Bulk conditioning was included to provide 115 Vac, 400 Hz to the secondary distributor.

A directive was sent from MSFC to Martin Marietta in May, 1986 to change the distributed power baseline from 115 Vac, three-phase, 400 Hz to 208 Vac, single-phase, 20 kHz. This, along with the 150 Vdc option, were to be the two distribution technologies which were to be developed. Schematics and previously developed equipment lists were updated to reflect this change to the 20 kHz baseline.

2.4 Network Concept Selection

The MSFC breadboard configuration was a combined effort of this contract and the of the Space Station Common Module Power Management and Distribution (SSM/PMAD) contract. A block diagram of the ring-bus configuration which was developed for the MSFC 20 kHz distribution breadboard is shown in Figure 2.4-1.

This configuration utilizes a dual ring bus driving two power distribution and control units (PDCU). Each PDCU contains three remote bus isolators (RBI's), two remote controlled circuit breakers (RCCB's), six-3 kW remote power controllers (RPC's), and twelve sensor sets. Each PDCU is capable of providing power to six load centers. A load center distributes power directly to user loads via 1 kW RPC's which can be cross-strapped to provide redundant load power.

A star-bus configuration (Figure 2.4-2) has been developed to distribute 120 Vdc (formerly 150 Vdc) in a separate MSFC breadboard. In the star-bus configuration, load centers are fed directly via RBI's and 3 kW RPC's from the PDCU's. This star-bus configuration is the present baseline for the +120 Vdc distribution system and has been developed as a working breadboard at MSFC.

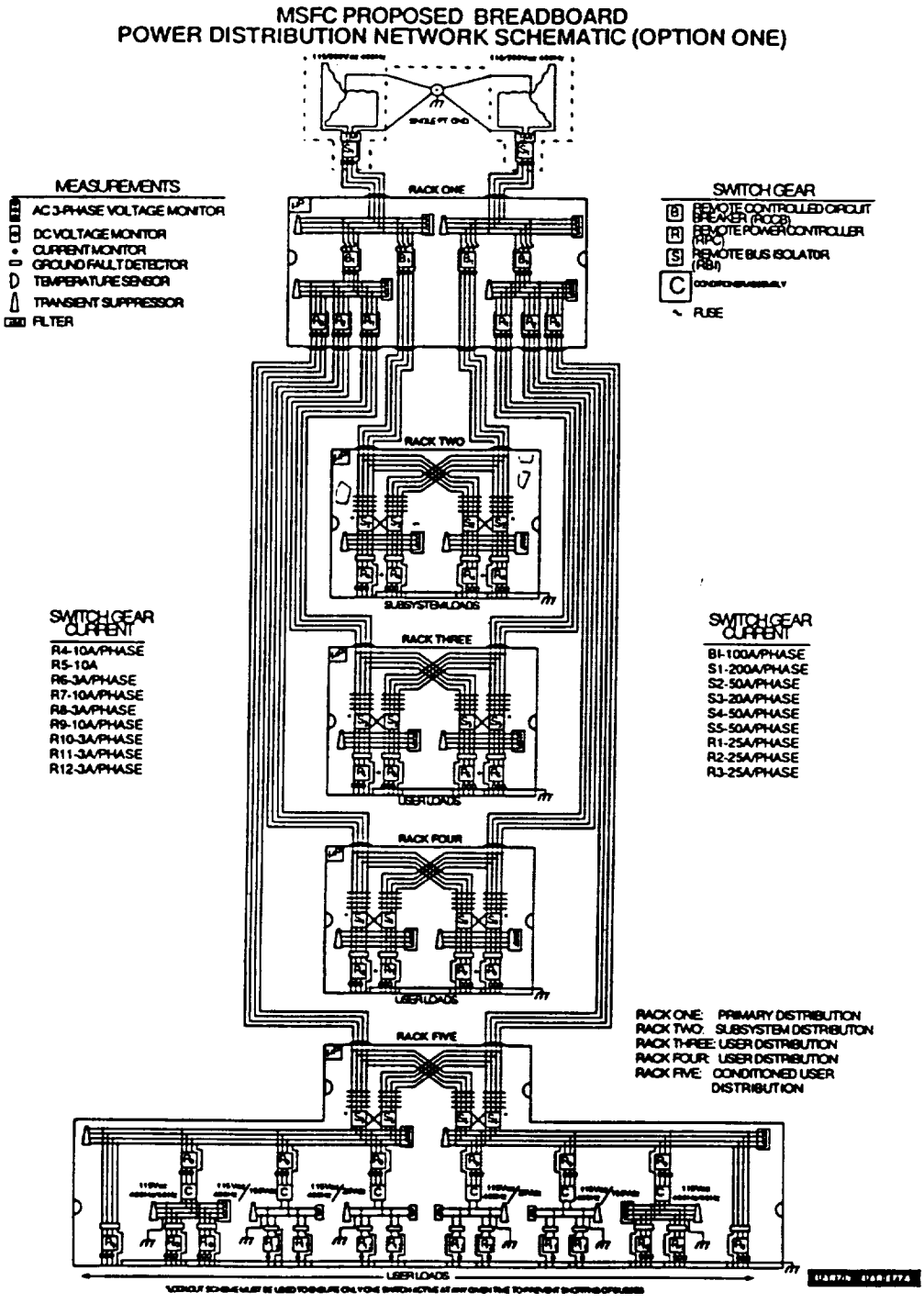

Figure 2.3-1 Option 1 Breadboard

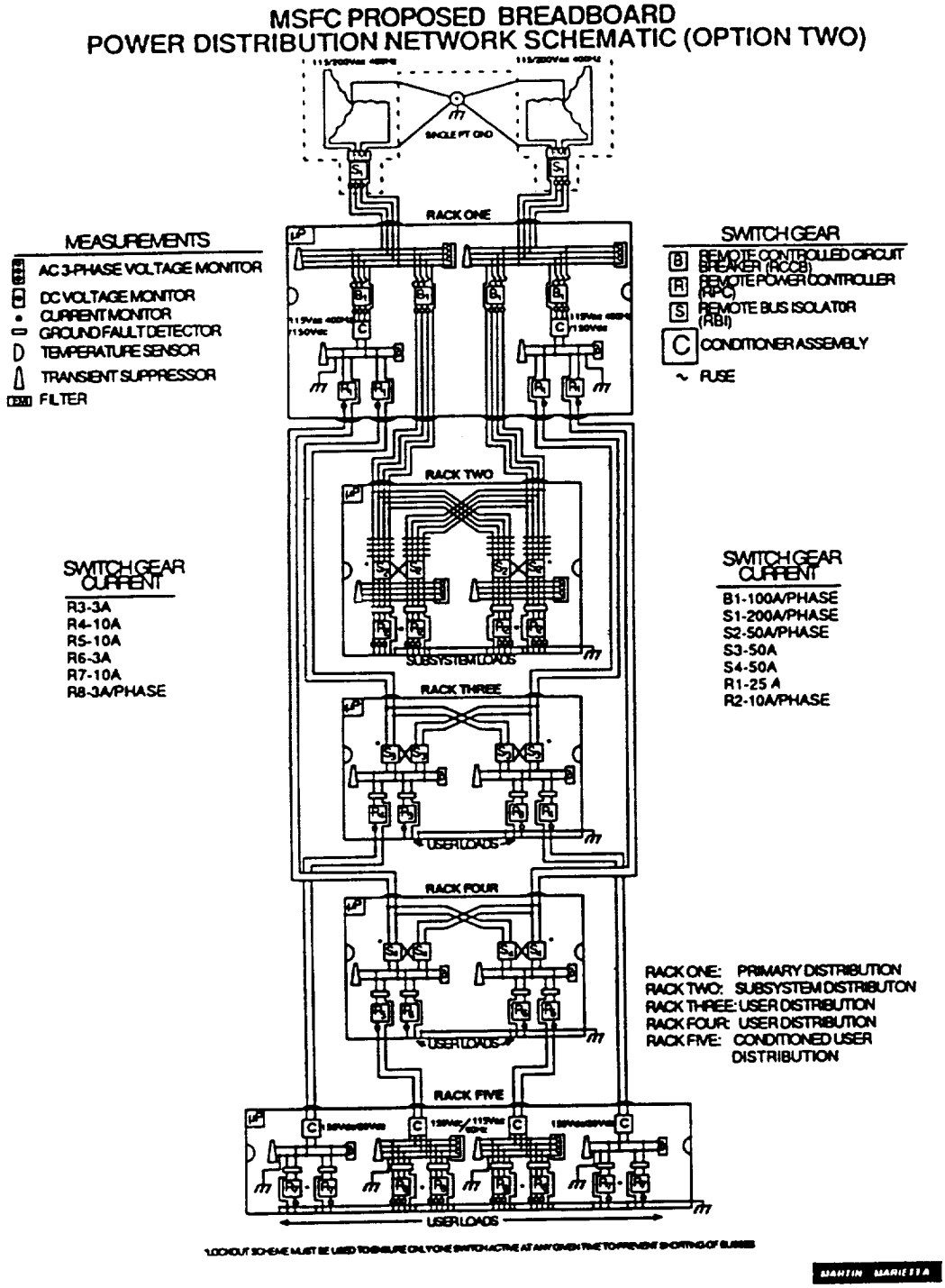

Figure 2.3-2 Option 2 Breadboard

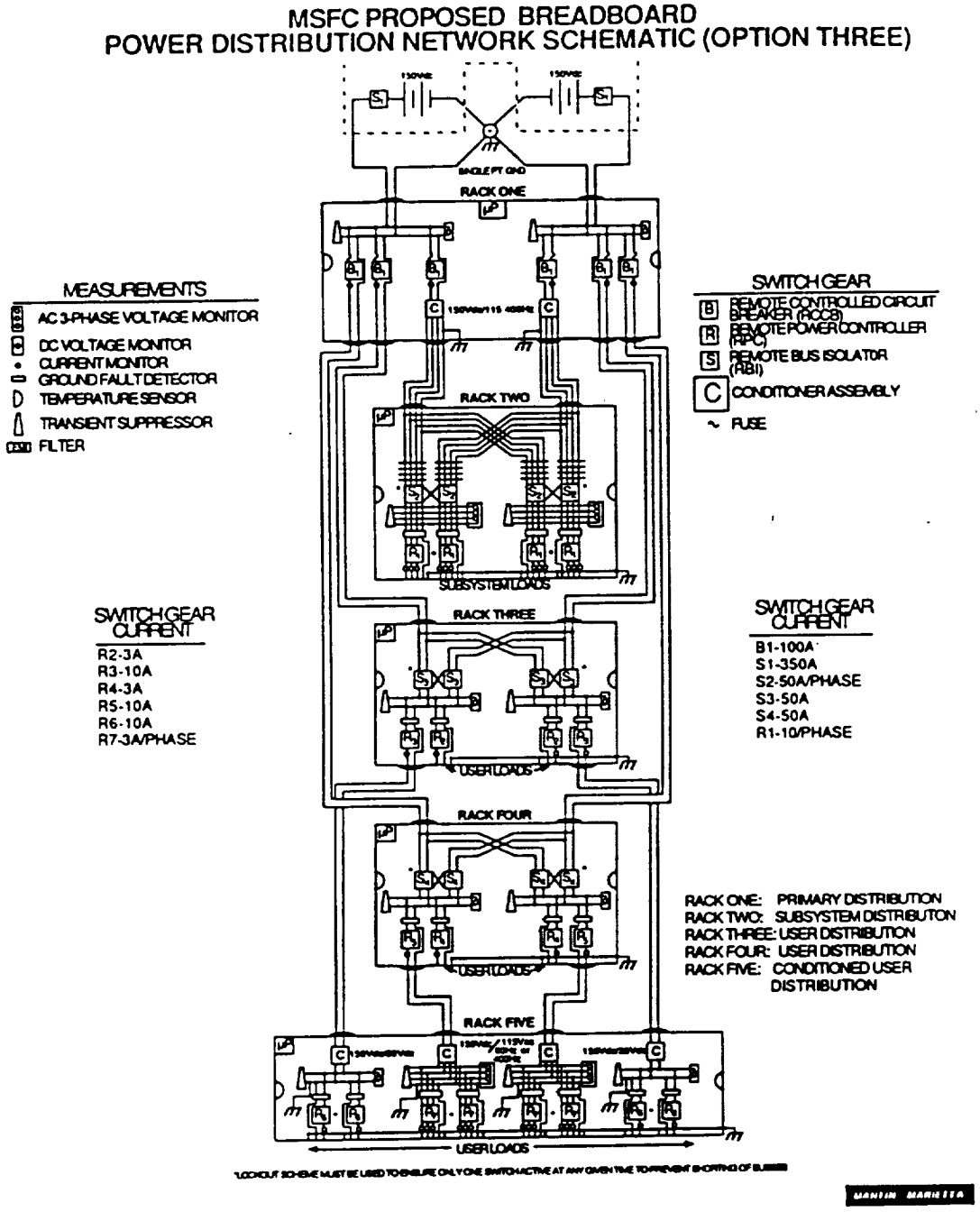

Figure 2.3-3 Option 3 Breadboard

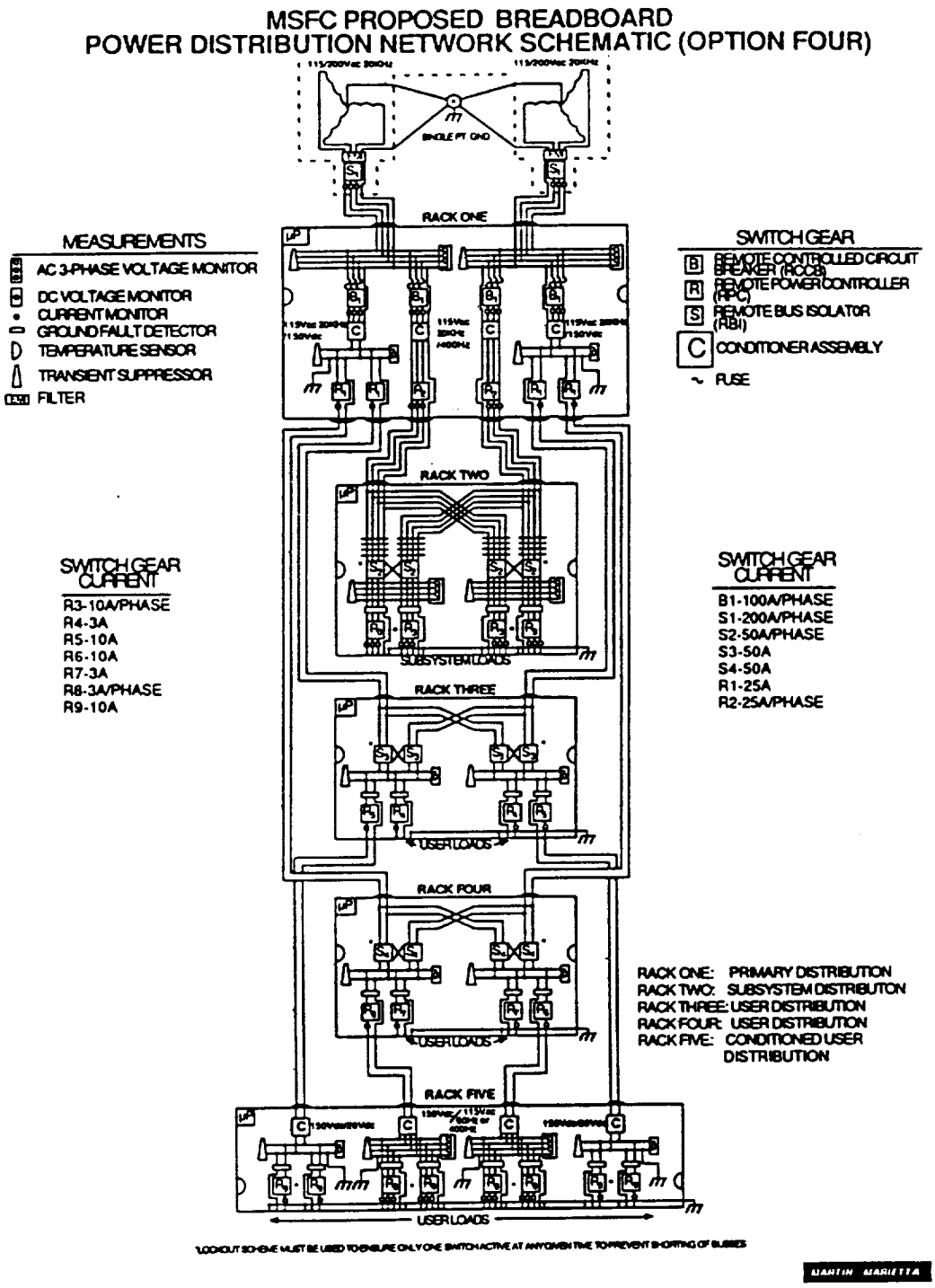

Figure 2.3-4 Option 4 Breadboard

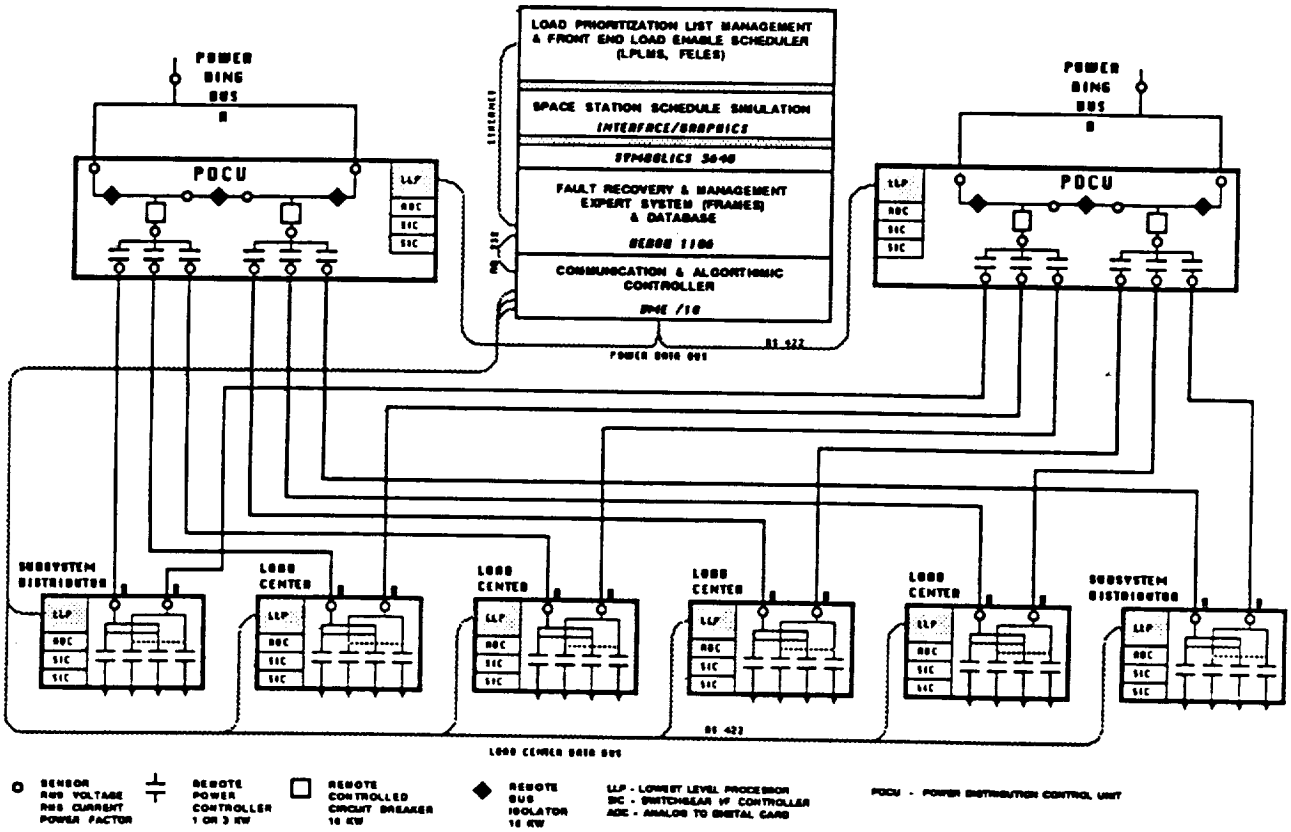

Figure 2.4-1 Ring Bus Configuration

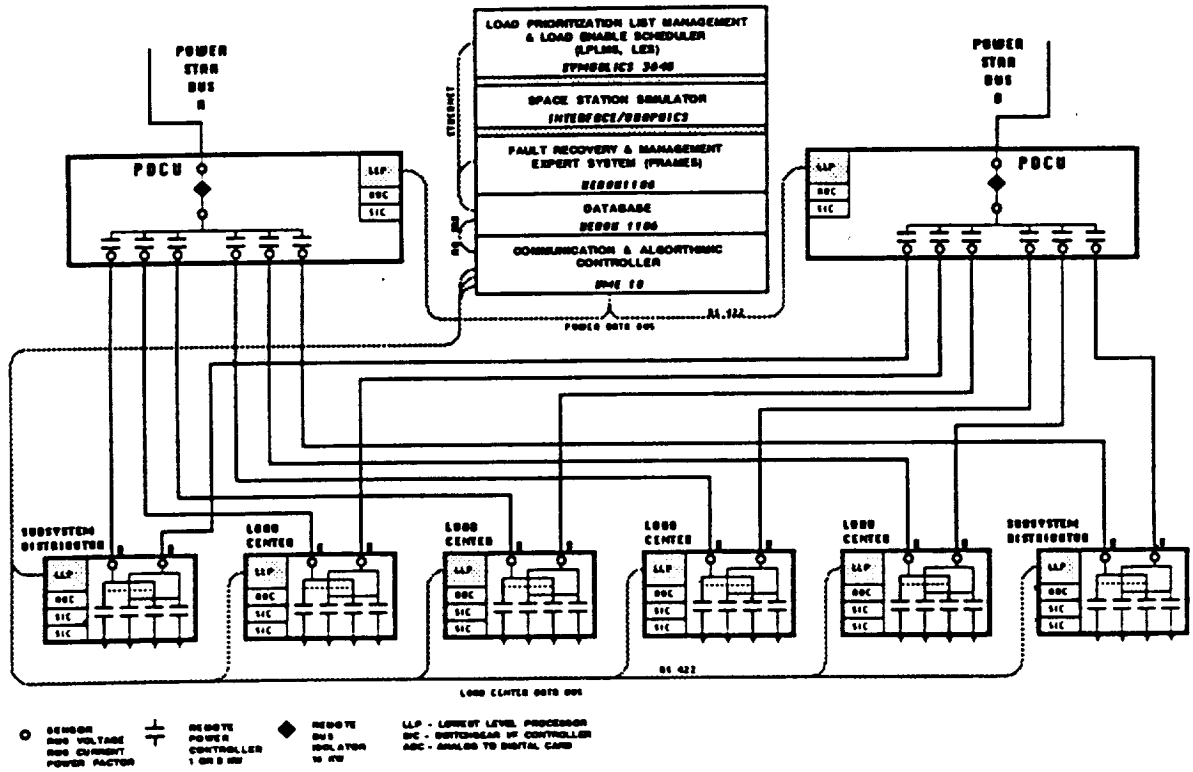

Figure 2.4-2 Star Bus Configuration

3.0 TASK II

Hardware Selection

The types and quantities of deliverable hardware which was selected to be incorporated into the MSFC breadboard is listed in Table 3.2-1. This list has been compiled and revised throughout the history of the contract. The original list was developed based on the breadboard topology selected, the original contract value, and the estimated cost of the individual hardware items. This original list was revised several times throughout the history of the program through a series of add-on and change-order proposals.

3.1 Technology Readiness Assessment

A technology readiness assessment report was developed during Task 2 which identified pieces of equipment requiring development effort to support the Space Station phase C/D effort. Equipment lists were developed from the previously selected network schematics. Additionally, functional requirements for the network equipment as well as other requirements which affected the suitability of specific items for use on the Space Station program were identified. A copy of this technology readiness report can be found in Appendix I.

Table 3.2-1 MSFC Breadboard Hardware (as of July, 1990)

Hardware Assembly	Number of Units
Remote Power Controller (RPC)	
AC 1 kW	20
AC 3 kW	12
DC 1 kW	35
DC 3 kW	15
Remote Controlled Circuit Breaker (RCCB)	
AC 10 kW	9
DC 10 kW	6
Remote Bus Isolator (RBI)	
AC	4
DC	2
Generic Controller Circuit (GC)	80
Switchgear Interface Controller (SIC)	14
Analog-to-Digital Card (A/D)	9
Card Cage	5
Test Tool	1
Temperature Sensor	40
Voltage Sensors	
DC 120 V	42
AC 208 V, 20 kHz	32
Current Sensors	
DC 15 A	12
DC 50 A	16
DC 100 A	17
Transorbs	15
SIC-LLP Interface Cables	15

4.0 TASK III

Hardware Advanced Development and Verification Tests

This section describes the requirements and design of each individual hardware assembly developed on the Space Station Common Module Network Topology and Hardware Development Program. Assembly requirements were derived based on the SSM/PMAD requirements developed during Task I and on the selected SSM/PMAD network concepts. Basic requirements and simplified design block diagrams are included in Section 4 for each assembly. Appropriate appendices have been added to include equipment specifications and product control drawings where applicable. These appendices are referenced in their proper assembly sections.

4.1 Switchgear Interface Controller (SIC)

4.1.1 SIC Requirements

The Switchgear Interface Control (SIC) Card is required to communicate with a Lowest Level Processor (LLP), 14 Generic Controller (GC) Cards, and an Analog to Digital (A/D) Card. The SIC must process 19 different commands sent from an LLP and return response data consistent with the LLP/SIC interface document found in Appendix II. Also, a SIC must communicate with 14 GC cards, each of which is capable of controlling and monitoring a Remote Bus Isolator (RBI), a Remote Controlled Circuit Breaker (RCCB), or a Remote Power Controller (RPC). Additionally, a SIC communicates with an A/D card and receives 16 voltage, current, and temperature sensor data inputs.

4.1.2 SIC Design

The SIC is designed to provide and receive command and data information from a lowest level processor, 14 GC cards, and an A/D card. This information is processed in a 6800 8-bit microprocessor programmed via a 2764 EPROM. A simplified block diagram of the SIC can be found in Figure 4.1.2-1.

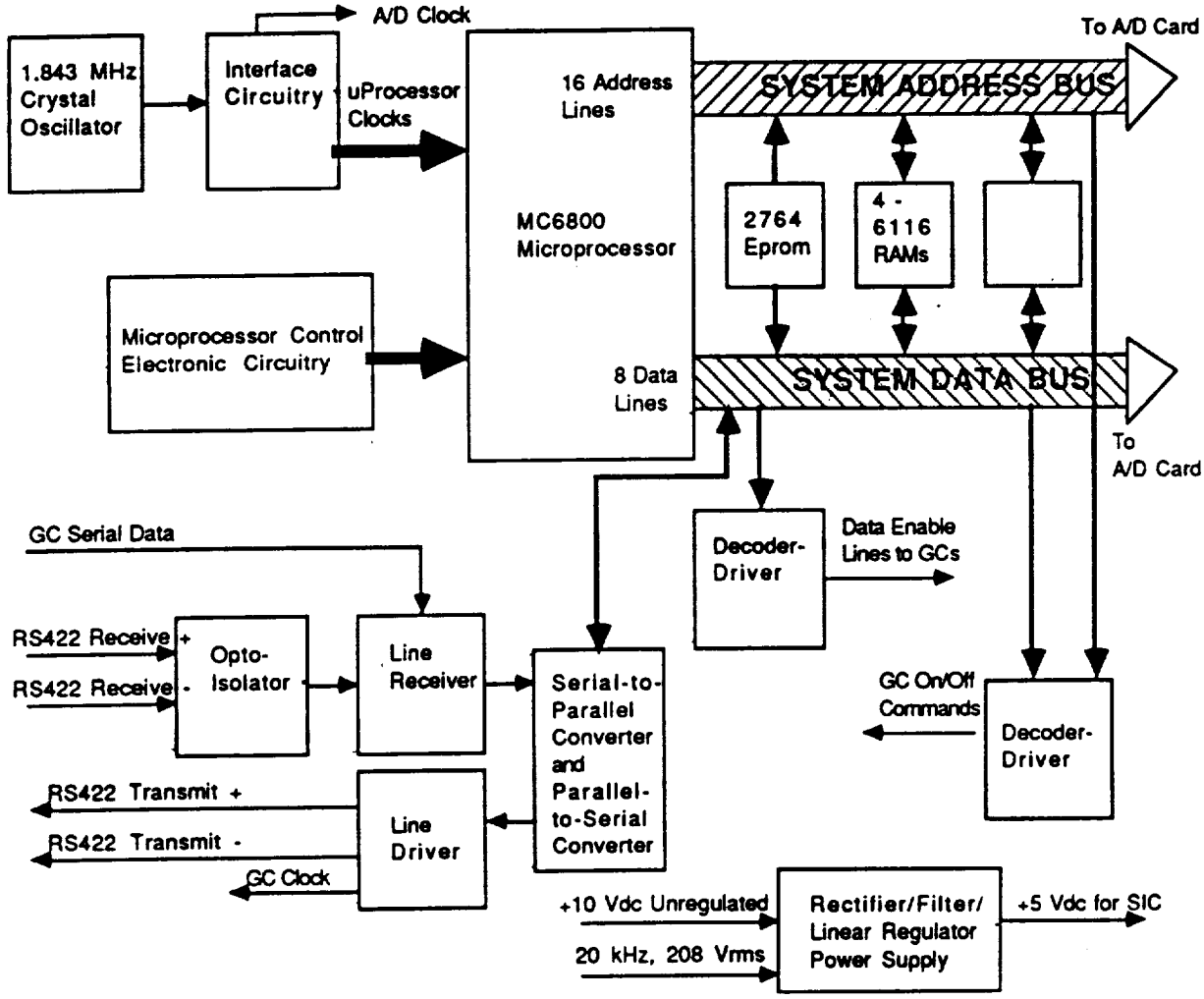

Figure 4.1.2-1 Switchgear Interface Controller Card

A SIC communicates serially with an LLP via optically-isolated RS-422 transmit and receive lines. The serial data that is received by the SIC is passed to a serial-to-parallel (8-bit) converter and transferred to the system data bus. Outgoing data from the SIC to LLP is transferred in the reverse order - first through a parallel to serial converter and then through a line driver to an optically-isolated receiver on the LLP. Data transfer occurs at the system clock rate of 640 kHz. A copy of the 19 different LLP to SIC command and response formats may be found in the SIC to LLP Interface Document in Appendix II.

A SIC also communicates serially with up to 14 GC cards. The SIC provides the GC cards with Data Enable, ON/OFF, and system clock inputs. The GC provides the SIC with serial data including switch status, fault, and current level information.

Communication between an A/D card and a SIC occurs directly on the system address and data busses. The SIC also provides the A/D card with system clock and interface read/write control lines.

The SIC uses a Motorola 6800 8-bit microprocessor to control system I/O, store data, and process commands. The compiled assembly code is contained on a 2764 EPROM and is found in assembly drawing #849NWT31126. The assembly code contains over 3000 lines of code and is compiled by a 2500 A.D. 6800 MacroAssembler. The resulting compiled object code is linked to create the executable binary file that resides on the EPROM.

4.2 Generic Controller (GC) Card

4.2.1 GC Requirements (Original)

A Generic Control (GC) Card is required to control the switching operation of a 20 kHz or DC RBI, RCCB, or RPC and return switch status information to the SIC. The GC card receives command data information from a SIC and "decides" whether or not to command a switch on or off (according to the Truth Table in 4.2.1-1). Additionally, the GC card processes analog signal information passed to it from a switch and decides when to "trip" a switch. Conditions which

warrant the GC tripping off a switch are Under Voltage, Over Current (I^2t), Surge Current, Ground Fault, and Over Temperature conditions. Additionally, an Over Temperature warning, a current limit switch turn on processor, and zero voltage and current crossing detectors are present on the GC. Values at which each of these conditions occur are listed in Table 4.2.1-2.

SIC to GC INPUTS		
ON	OFF	SWITCH STATUS
0	0	ON (HARDWARE ERROR)
0	1	ON
1	0	OFF
1	1	NO CHANGE

Table 4.2.1-1 GC Card Truth Table Requirements

Condition	Values
Under Voltage	85% of Line Voltage
Over Current (I^2t)	115% RMS Current
Surge Current	400% RMS Current
Ground Fault	50 mA for 40 mS
Over Temperature Trip	125 Degrees Celsius
Over Temperature Warning	100 Degrees Celsius
Current Limit Turn On	130% RMS Current

Table 4.2.1-2 GC Card Processor Trip Level Requirements

4.2.2 GC Design (Original)

The Generic Card (Figure 4.2.2-1) is the controller board for any type of AC or DC switch (RBI, RCCB, or RPC). Each GC Card is capable of controlling and monitoring one switch, and can communicate serial switch information to one of two possible SIC cards. The GC takes analog signal processor, switch status, switch configuration, and SIC command information through a state machine (ALTERA Programmable Logic Element and 2764 EPROM) to control the switching operation of a switch. The GC provides the SIC card with serial data via an analog-to-digital converter and a parallel-to-serial converter.

The analog processors which are present on the GC can be found in Table 4.2.2-1. The output of each of these processors provides inputs to the state machine and describes which, if any, trips have occurred on the switch. A block diagram schematic of each of the analog processors listed in Table 4.2.2-1 can be found in Figure 4.2.2-2.

Under Voltage	Over Temp Trip	I^2t Trip
Zero Voltage Xing	Over Temp Warning	Surge Current Trip
Ground Fault	Zero Current Xing	Inrush Over Current

Table 4.2.2-1 Analog Signal Processors

The GC receives switch status information from the switches in the form of either or both a mechanical (relay) and a main (solid-state) status. The GC uses pull-up resistors via the switchgear to develop the proper digital signal which feeds the state machine (Figure 4.2.2-3).

The GC card state machine operation is dependent upon which type of switch it is controlling. Figure 4.2.2-4 shows the various configurations for AC and DC RBIs, RCCBs, and RPCs. Each of the various configure lines influences the path that the state machine takes during its operation. Table 4.2.2-2 lists each line which determines a switch's configuration and describes what each

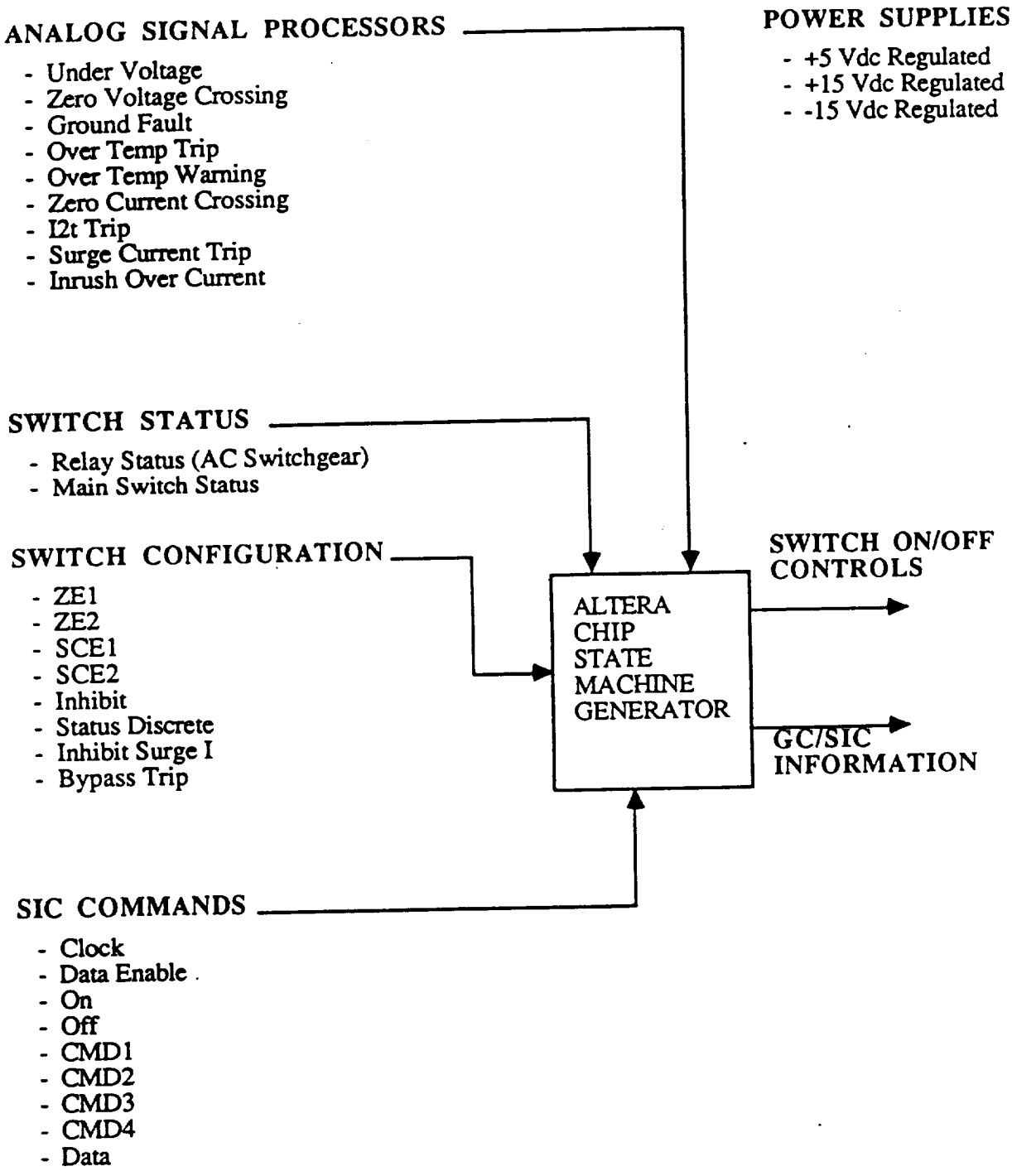

Figure 4.2.2-1 Generic Controller Card

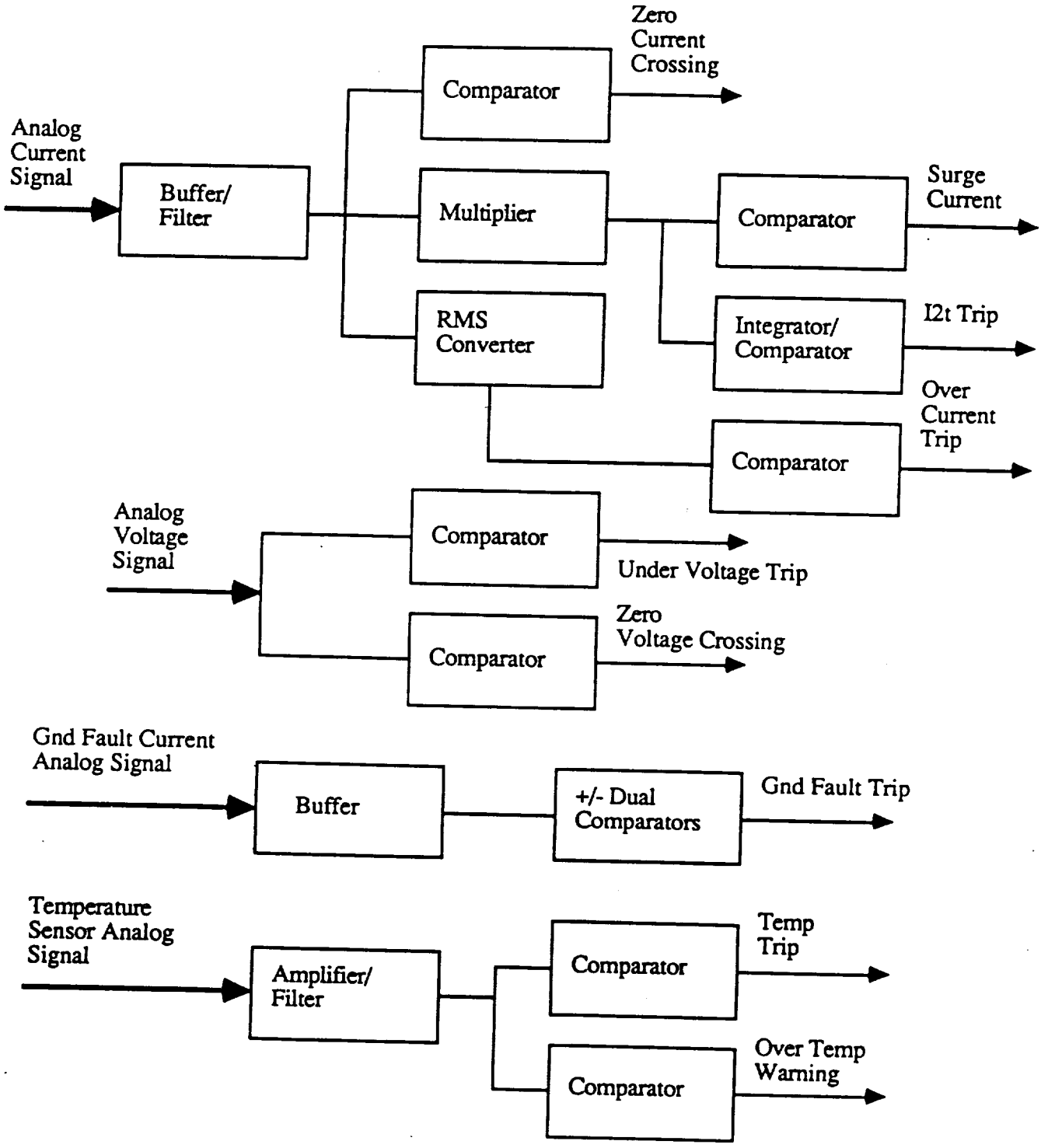

Figure 4.2.2-2 GC Card Analog Processors

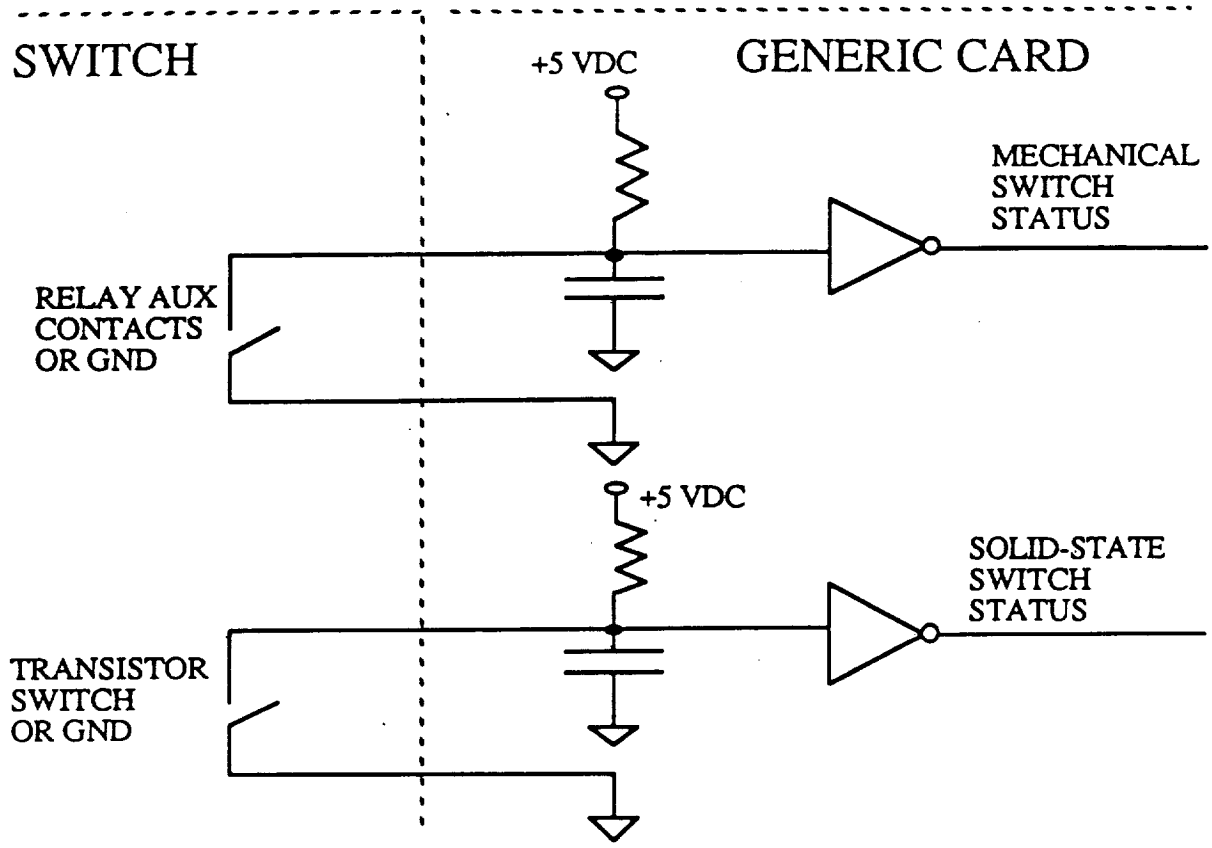

Figure 4.2.2-3 Generic Card Switch Status Circuitry

CONFIGURATION LINE	AC RBI	AC RCCB	AC RPC	DC RBI	DC RCCB	DC RPC
ZE1	ON	ON	OFF	ON	OFF	OFF
ZE2	ON	ON	OFF	ON	OFF	OFF
SCE1	ON	ON	OFF	ON	OFF	OFF
SCE2	ON	ON	OFF	ON	OFF	OFF
INHIBIT	OFF	OFF	OFF	OFF	OFF	OFF
INHIBIT SURGE I	ON	ON	OFF	ON	ON	OFF
INTWICE	ON	ON	OFF	ON	ON	ON
BYPASS TRIP	ON	OFF	OFF	ON	OFF	OFF
STATUS DSCRT	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
	NOTE: 'ON' is GND AND 'OFF' IS +5 VDC					

Figure 4.2.2-4 Generic Card Configurations

one does. Additionally, several of these lines are not currently being utilized and are identified as such.

Configuration Line	Description
ZE1	Not Used
ZE2	Not Used
SCE1	Smart Contactor Enable (Not Used)
SCE2	Smart Contactor Enable (Not Used)
Inhibit	When 'ON', the switch is inhibited Normally tied to +5, but can be used with 'status discrete' for cross-strapping purposes
Inhibit Surge I	When 'ON', the switch will not trip on a surge current trip
Intwice	When 'ON', the switch will not get a 'second chance' to turn back on when a current trip occurs
Bypass Trip	When 'ON', the switch will not trip off on any form of trip (over current, under voltage, over temp, gnd fault, etc.). Used only on an AC or DC RBI.
Status Discrete	Used in conjunction with Inhibit - used when switches are cross-strapped (a failure of one switch causes another to turn on)

Table 4.2.2-2 - Switch Configuration Lines and Descriptions

The GC Card state machine utilizes 13 separate states to control the switching operation of a switch. This state machine resides internal to the ALTERA chip. The various states are decoded and switches are turned on and off via a 2764 EPROM.

Upon any given power up or if an off command or inhibit is received, the ALTERA chip enters state 0 and all switches get commanded off. The remaining state machine sequencing is described in Figure 4.2.2-5.

4.2.3 GC Requirements (DC only GC)

Following the decision to develop a +120 Vdc breadboard in January, 1989, a generic controller card was designed and de .oped which was required to control only DC switchgear. The functional requirements of the new DC-GC are identical to those of the original GC with the exception that the new GC is required to control only DC switchgear.

4.2.4 GC Design (DC only GC)

The DC-only Generic Card (Figure 4.2.4-1) is the controller board for any type of DC switch (RBI, RCCB, or RPC). Each DC-GC Card is capable of controlling and monitoring one switch, and can communicate serial switch information to one of two possible SIC cards. The GC takes analog signal processor, switch status, switch configuration, and SIC command information through a state machine (ALTERA Programmable Logic Element) to control the switching operation of a switch. The GC provides the SIC card with serial data via an analog-to-digital converter and a parallel-to-serial converter.

The analog processors which are present on the DC-GC can be found in Table 4.2.4-1. The output of each of these processors provides inputs to the state machine and describes which, if any, trips have occurred on the switch. A block diagram schematic of each of the analog processors listed in Table 4.2.4-1 can be found in Figure 4.2.4-2.

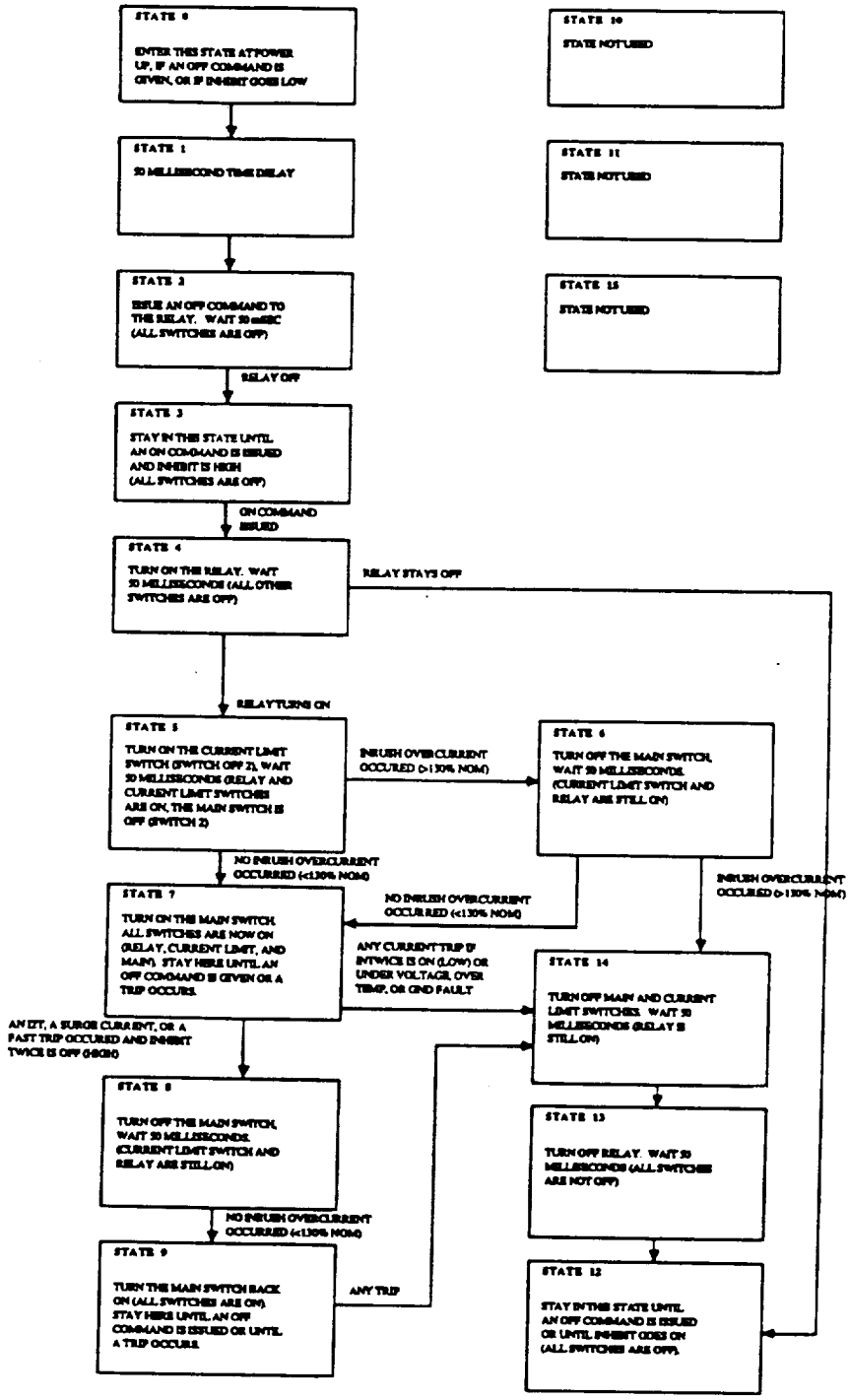

Figure 4.2.2-5 GC Card State Machine

Under Voltage	Over Temp Trip	I^2t Trip
Over Temp Warning	Surge Current Trip	Ground Fault*
	Inrush Over Current	

* Present on the DC GC but not implemented on the DC RPCs

Table 4.2.4-1 DC-GC Analog Signal Processors

The DC-GC receives switch status information from the switches in the form of a switch type signature (1kW RPC, 3 kW RPC, or RBI) and a main (solid-state) switch status. The DC-GC uses pull-up resistors via the switchgear to develop the proper digital signal which feeds the state ine (Figure 4.2.4-3).

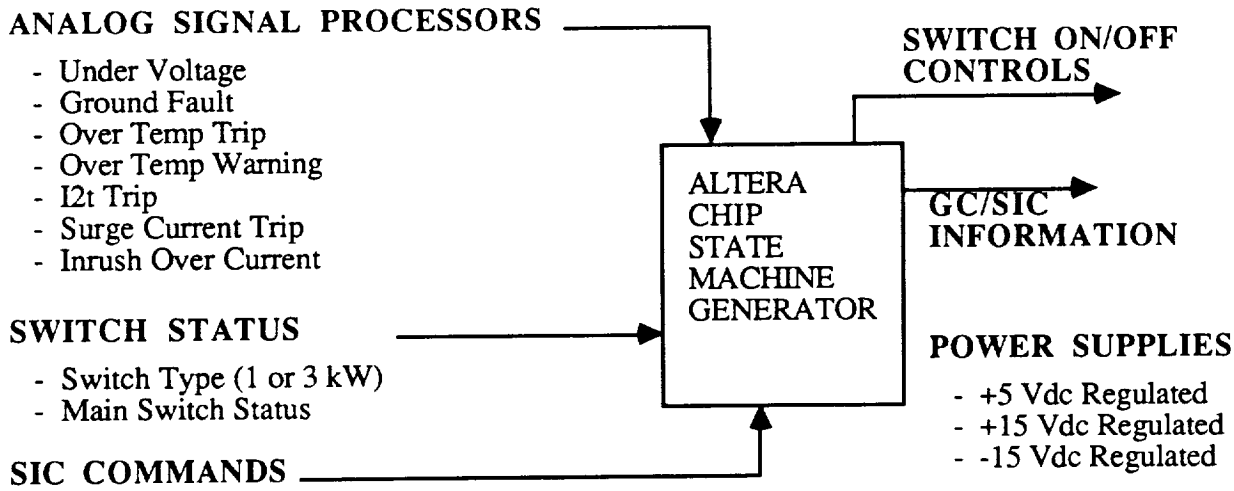

Figure 4.2.4-1 DC-Generic Controller Card

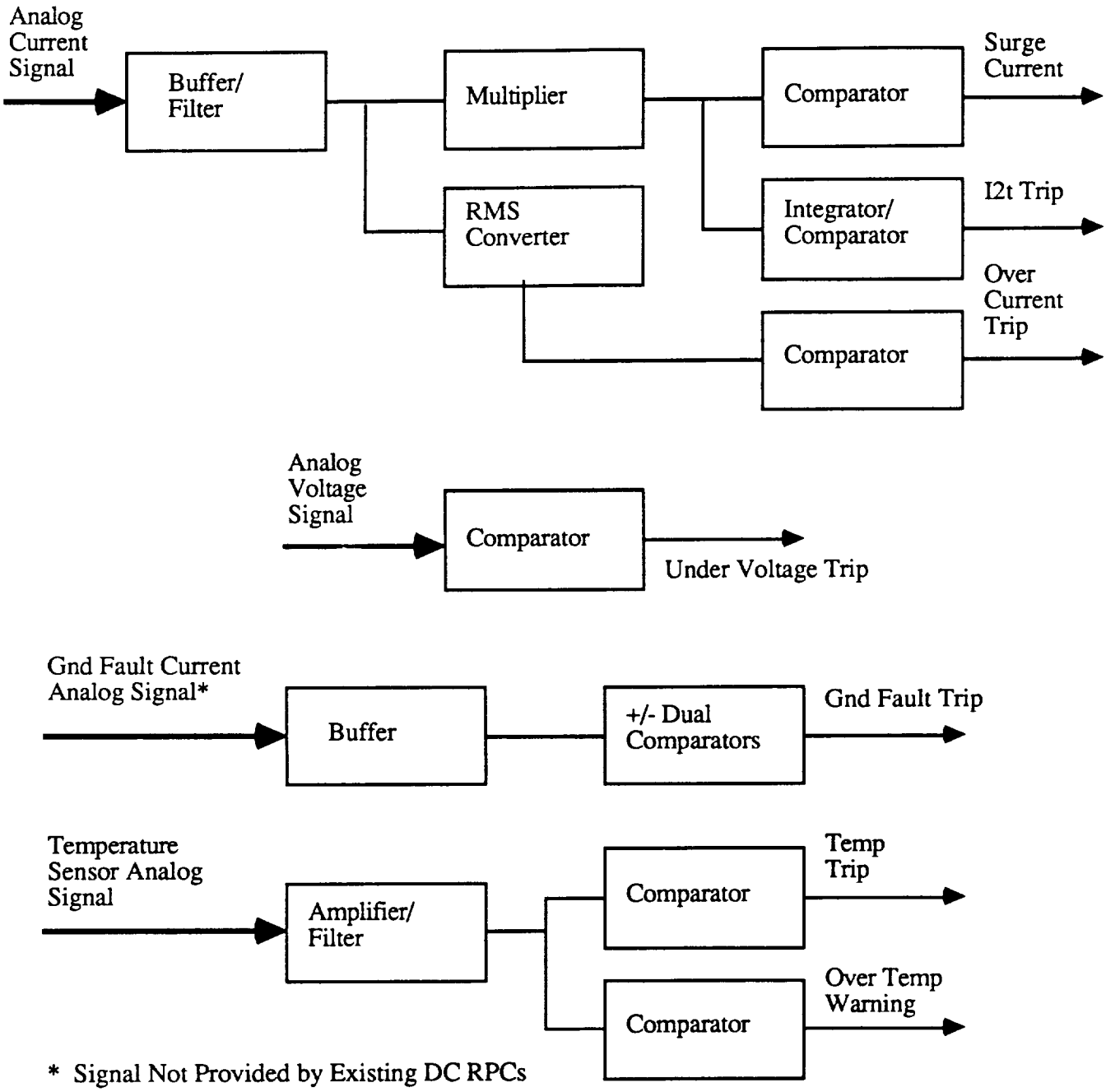

Figure 4.2.4-2 GC Card Analog Processors

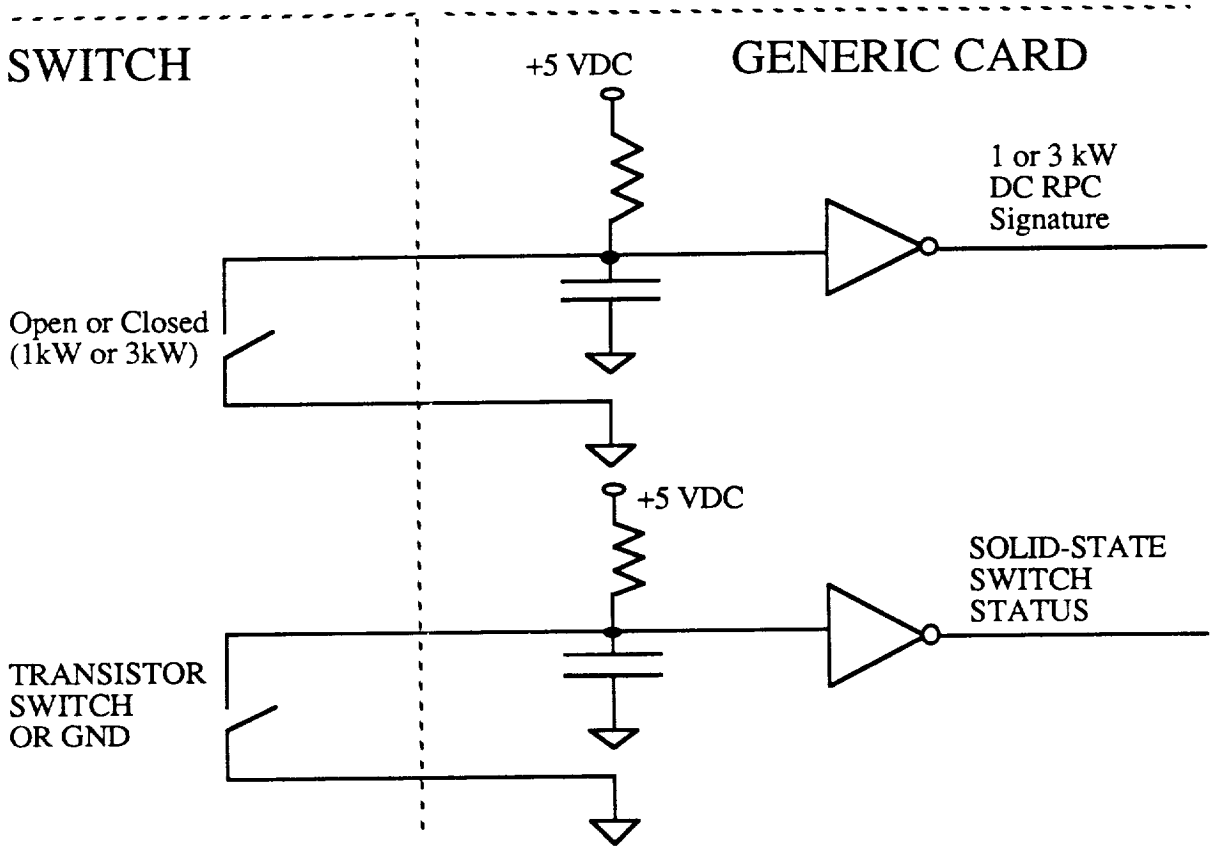

Figure 4.2.4-3 Generic Card Switch Status Circuitry

The DC-GC Card state machine utilizes 6 separate states to control the switching operation of a switch. This state machine resides internal to the ALTERA chip.

Upon any given power up or if an off command or inhibit is received, the ALTERA chip enters state 0 and all switches get commanded off. The remaining state machine sequencing is described in Figure 4.2.4-4.

4.3 Analog to Digital (A/D) Card

4.3.1 A/D Requirements

The Analog to Digital (A/D) Card is required to accept 16 voltage, current, and temperature sensor inputs and return proportional digitized information to the SIC card. The A/D card processes the analog sensor inputs and returns digitized RMS voltage, RMS current, average voltage, average current, frequency, average power, instantaneous power, power factor, and temperature data to the SIC card. The required sensor input levels to the A/D and their 8-bit equivalent which gets passed to the SIC can be found in Table 4.3.1-1.

Inputs Used	Processors	Digital Input Range Analog Input Range	(Base 10)
Voltage (V)	RMS, Ave., Freq.	-10V to 10V	0 to 255
Current (I)	RMS, Ave.	-10V to 10V	0 to 255
V & I	Inst. Pwr, Ave Pwr., Pwr Factor	-10V to 10V	0 to 255
Temperature	Temperature	2342 to 8806 Ohms	0 to 255

Table 4.3.1-1 - Required A/D Card Sensor Inputs, Processors and Ranges

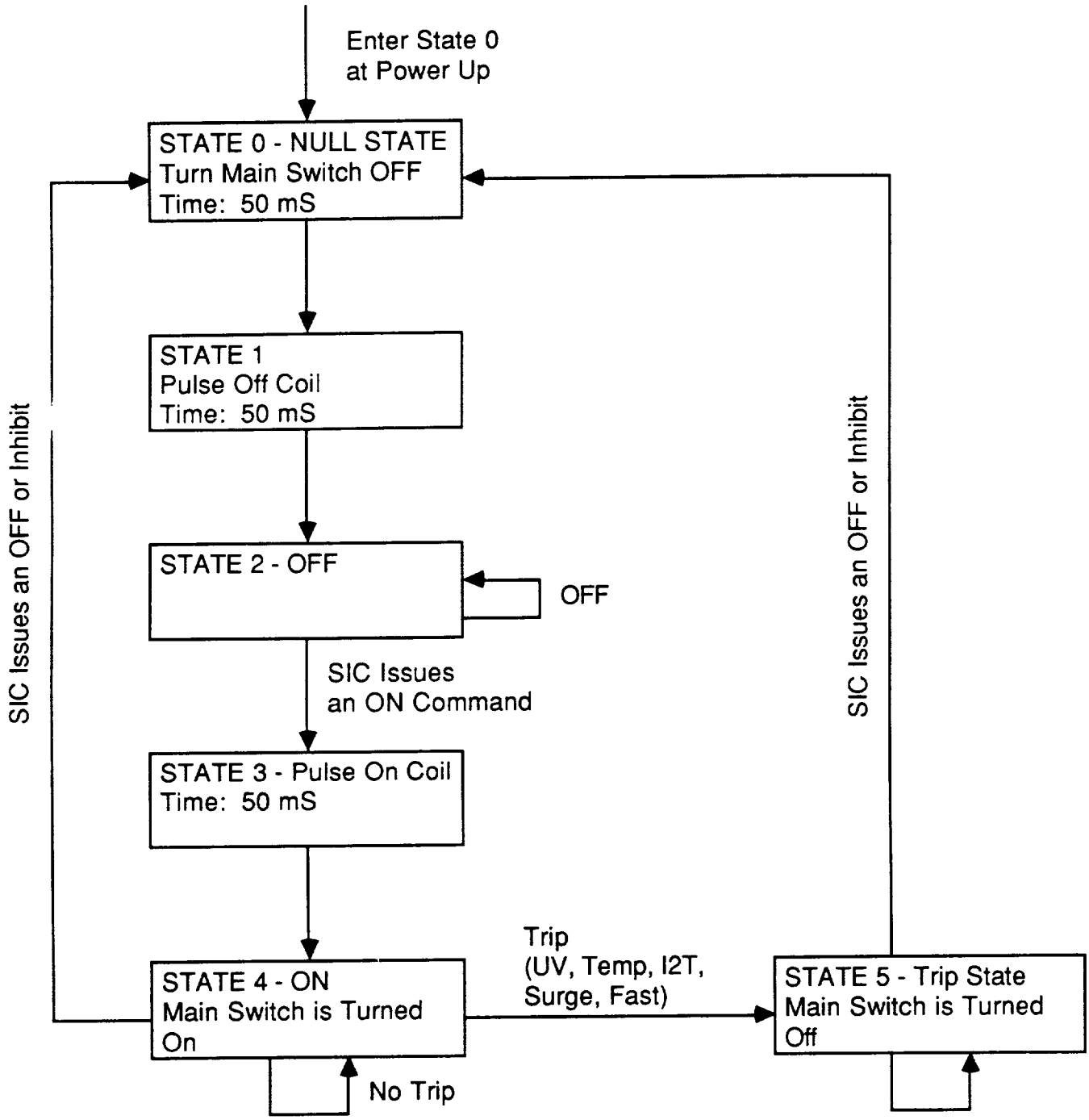

Figure 4.2.4-4 DC-GC Card State Machine

4.3.2 A/D Design

The analog to digital card accepts voltage, current, and temperature analog inputs and returns eight-bit digital information to the SIC. A functional block diagram of the A/D card is shown in Figure 4.3.2-1.

Current and voltage sensor inputs are accepted and passed through MC34004 difference amplifiers to allow for proper signal referencing and isolation. The (16) voltage and (16) current sensor signals are then passed through an analog multiplexer. The proper channel is selected via the SIC address bus when the SIC requests data from a given sensor. Several analog processors reside on the output of the multiplexers including amplifier/integrators, RMS converters, and an analog multiplier. These chips process the appropriate analog signal which allows average, RMS, and power readings to be available to the A/D converter. Following these analog processors is another multiplexer stage which allows the SIC to select what type of reading it desires from the A/D card (voltage, current, temperature, average, RMS, etc.). The proper channel is selected via the SIC address bus as with the previous multiplexer.

Temperature sensor inputs are accepted and fed into the inverting input of a single-ended MC34004 operational amplifier. Any variation in the impedance of the temperature sensor results

in a change in the output voltage of the operational amplifier. This amplifier inputs to the second stage multiplexer as described above.

The selected output of the second multiplexer is input to an SI8601 analog-to-digital converter which is referenced at 5 VDC. The gain of each amplifier stage feeding the A/D converter is set to input 2.5 VDC at 100% sensor rating (5 V analog at the input to the A/D card). This allows the A/D card to have a +/- 200% sensor rating range.

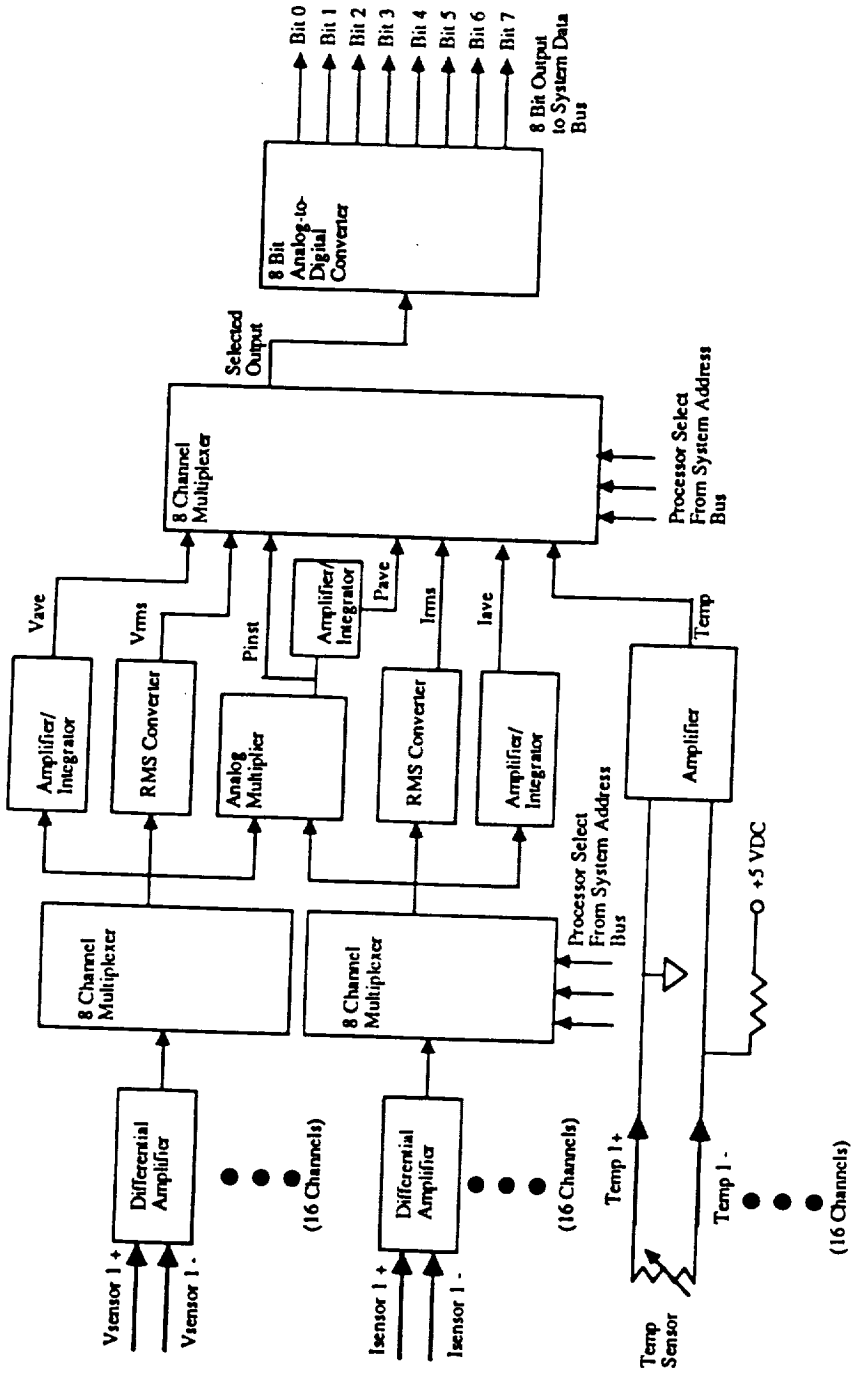

Figure 4.3.2-1 Analog to Digital Card

4.4 AC Remote Power Controller (RPC)

4.4.1 AC RPC Requirements

An AC Remote Power Controller (RPC) is required to provide 5A (1kW) or 15A (3kW) at 208 Vrms, 20kHz to any resistive, capacitive, or inductive load. The switch is SPST with a main solid state switch, a parallel current limiting switch, and a relay isolator. Commanding on and off of the RPC is controlled by a GC card.

The RPC provides the GC with analog current, voltage, ground fault, and temperature sensor inputs. Additional switch telemetry data which is passed to the GC includes an auxiliary relay contact and a solid-state switch status indicator.

A "Fast Trip" shutdown circuit is required to be present on the RPC power stage. If a 400% peak current is detected by the RPC, the main solid state switch immediately shuts off (<1uS) and the RPC current limits the fault. Control of the RPC is returned to the GC card for further processing once the main solid state switch has turned off.

4.4.2 AC RPC Design

The AC RPC (Figure 4.4.2-1) is designed to be a self-protecting SPST switch controlled from a GC card. The main parts that comprise the RPC are the switching unit, the "fast trip" circuitry, the analog sensors, and various power supplies.

The switching unit (developed by Leach Corp.) is comprised of a magnetically latching relay, a main solid state switch, and a parallel current limiting switch; all controlled from the GC card. The latching relay provides both power and return isolation to the load when the RPC is off. The relay has a +24 Vdc coil and is magnetically latching with an auxiliary contact which provides relay status information to the GC card. The main solid state switch is comprised of parallel MOSFETS and is in series with the main relay contracts. Parallel MOSFETS are required to

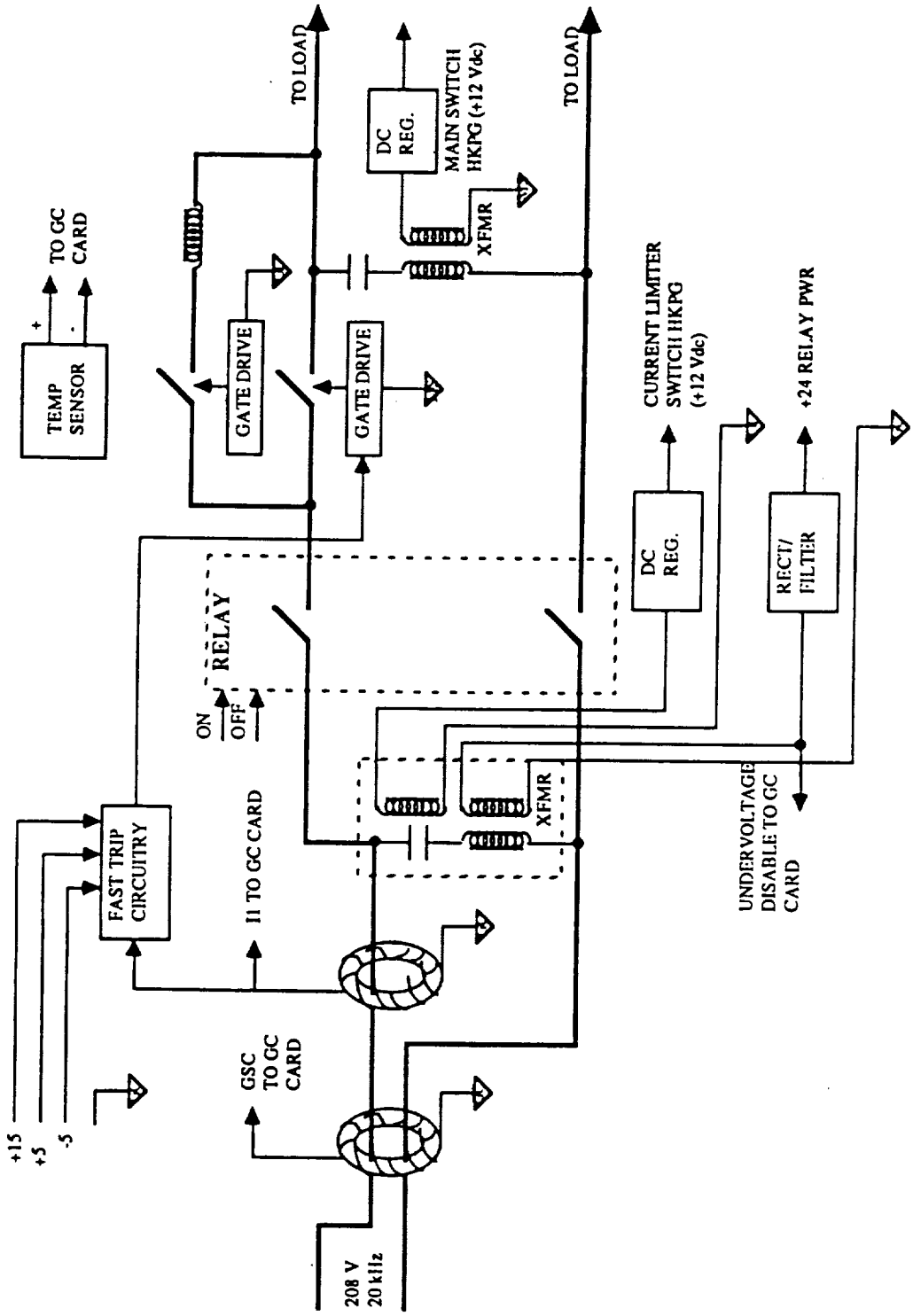

Figure 4.4.2-1 AC Remote Power Controller

provide sufficient carrying capability and to reduce the MOSFET on resistance. This prevents large voltage drops from appearing across the RPC (<3 Vrms). The main solid state switch provides zero voltage turn on and zero current turn off switching for the RPC.

In parallel with the main solid state switch is a solid state current limiting switch. The current limiting switch is comprised of parallel MOSFET switches in series with an inductor. The inductor provides sufficient impedance at 20 kHz to limit any inrush or fault current to 130% RMS. The main and current limiting solid state switches both have optically isolated gate drives which significantly reduce cross-talk noise. The GC card controls the main and current limiting switches such that they are never both on at the same time.

The "fast trip" circuitry detects peak currents exceeding 400% using zener diode sensing and fast transistor control. Any peak current exceeding 400% rated (positive or negative peak) cause the main solid state switch to immediately turn off (<1 uS), immediately causing the RPC to enter the current limiting mode. Additionally, the "fast trip" circuitry returns the status of the main switch. This fast trip circuitry provides inherent self-protection for the RPC.

The RPC provides the GC card processors with analog data as listed in Table 4.4.2-1. The GC card, after processing the analog signals, decides when a trip condition has occurred. The only trip condition which occurs directly on the RPC is the fast trip.

A number of separate power supply voltages and grounds are present on the RPC, as summarized in Table 4.4.2-2. The latching relay uses +24 Vdc developed on the secondary of a transformer at the input of the RPC to drive its coil. The secondary of the transformer is rectified and filtered; using a sufficiently large capacitor for energy storage in the event of a 20 kHz power line failure. Control of the relay is done by the GC card. The +12 Vdc current limiting switch housekeeping power is developed on the same transformer that the relay coil power is developed, using a separate ground reference. The +12 Vdc is developed via a rectifier-filter-linear regulator approach.

The +12 Vdc main solid state switch housekeeping power is developed on a second transformer that is "downstream" from the relay. This insures that housekeeping power is developed for the

main solid state switch only after the relay has been closed. A rectifier-filter-linear regulator is used to develop the +12 Vdc. Separate +5, +15, and -15 Vdc power is delivered from the GC card to power the fast trip circuitry.

Analog Signal	RPC Signal Level	GC Signal Level
Ground Fault	50 mA	0.50 Vrms
Under Voltage	85 % of 208 Vrms	9.0 Vrms
Current	100% Rated Current	1.0 Vrms
Temperature	100 C	-3.73 Vrms
Temperature	125 C	-3.98 Vrms

Table 4.4.2-1 RPC Analog Data Given to the GC Card

Voltage	Reference	Source	Load
+5	GC GND	GC Linear Regulator	Fast Trip Circuitry
+15	GC GND	GC Linear Regulator	Fast Trip Circuitry
-15	GC GND	GC Linear Regulator	Fast Trip Circuitry
+24	GC GND	RPC Rectifier/Filter	Relay Coil
+12	Main Switch GND	RPC Linear Regulator	Main Switch Hkpg
+12	CL Switch GND	RPC Linear Regulator	CL Switch Hkpg

Table 4.4.2-2 RPC Housekeeping Power Supplies and Loads

Martin Marietta has developed a preliminary equipment specification guide for a 20 kHz AC RPC (Appendix III). This unreleased document is an example of what format a formal equipment specification would undertake for a flight-type RPC. Included in this document are the controller card requirements which would reside as part of the RPC. This document was used as a guide in developing our 20 kHz breadboard RPCs but does not reflect our specific breadboard design.

4.5 AC Remote Controlled Circuit Breaker (RCCB)

4.5.1 AC RCCB Requirements

An AC Remote Controlled Circuit Breaker is required to provide 50A (10 kW) at 208 Vrms, 20 kHz to up to 3 fully-loaded 3 kW RPCs. The switch is SPST and consists of a large relay which switches both the positive and return sides of the 20 kHz. The RCCB may be switched 'hot'.

The RCCB must provide the GC with analog current sensor data and relay status information. Commanding on and off of the RCCB is controlled by a GC card.

4.5.2 AC RCCB Design

The AC RCCB (Figure 4.5.2-1) is designed to provide 20 kHz power for up to 3 fully-loaded 3 kW RPCs. The main parts that comprise the RCCB are the relay, the relay interface electronics, and the current transformer.

The relay is used as a single pole, double throw magnetically latching relay with 2 power contacts and an auxiliary contact used for relay status information. The relay is manufactured by Leach Corp., and has a current rating of 120 amps.

The relay interface electronics included protection diodes across the relay coils, an inductive kickback prevention diode for the +15 VDC supply from the GC Card, and an energy storage capacitor to insure rapid turn on and turn off of the relay.

The current transformer is designed to provide the GC Card with an analog voltage signal proportional to the AC RCCB current. An RCCB current exceeding 115% of rated (10 kW at 208 Vrms) will result in the GC Card 'tripping off' the AC RCCB.

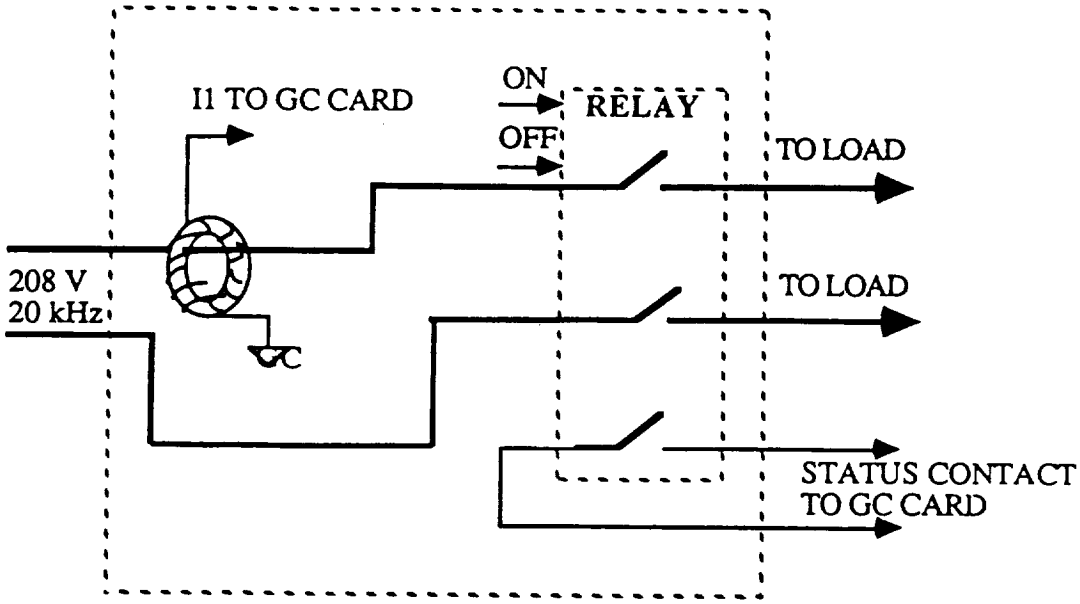

Figure 4.5.2-1 AC Remote Controlled Circuit Breaker

4.6 AC Remote Bus Isolator (RBI)

4.6.1 AC RBI Requirements

An AC Remote Bus Isolator is required to provide 15 kW, 208 Vrms at 20 kHz to RCCB switches. The switch is SPST and consists of a large relay which switches both the positive and return sides of the 20 kHz. The RBI can only be switched when the 20 kHz power is off.

The RBI must provide the GC card with relay status information only. Commanding the RBI on and off is controlled by a GC card.

4.6.2 AC RBI Design

The AC RBI (Figure 4.12.2-1) is designed to provide 20 kHz power to an AC RCCB. The main parts that comprise the RBI are the relay and the relay interface electronics.

The relay is used as a single pole, double throw magnetically latching relay with 2 power contacts and an auxiliary contact used for relay status information. The relay is manufactured by Leach Corp., and has a current rating of 120 amps.

The relay interface electronics included protection diodes across the relay coils, an inductive kickback prevention diode for the +15 VDC supply from the GC Card, and an energy storage capacitor to insure rapid turn on and turn off of the relay.

4.7 AC Voltage Sensor

4.7.1 AC Voltage Sensor Requirements

An AC voltage sensor is required to provide a differential isolated voltage input to one of 16 voltage channels present on an A/D card. The secondary voltage is required to be 5.00 +/- 0.25 Vrms for a prim input of 208 Vrms, 20 kHz.

4.7.2 AC Voltage Sensor Design

The AC voltage sensor (Figure 4.7.2-1) is comprised of a primary DC blocking capacitor, a step-down transformer, and appropriate burden resistors to provide 5 Vrms out for 208 Vrms in.

A 0.01 uF, 600V capacitor is in series with the transformer primary winding to prevent any DC bias from appearing across the winding. A net resulting volt-second imbalance from the dc bias across the transformer could result in the transformer saturating, resulting in the failure of the sensor.

The transformer used in the sensor is a Corona Magnetics 1383B. The primary winding has 650 turns and the secondary winding has 46 turns.

Appropriate secondary voltage divider resistors are chosen such that the output voltage is 5 Vrms for an input of 208 Vrms.

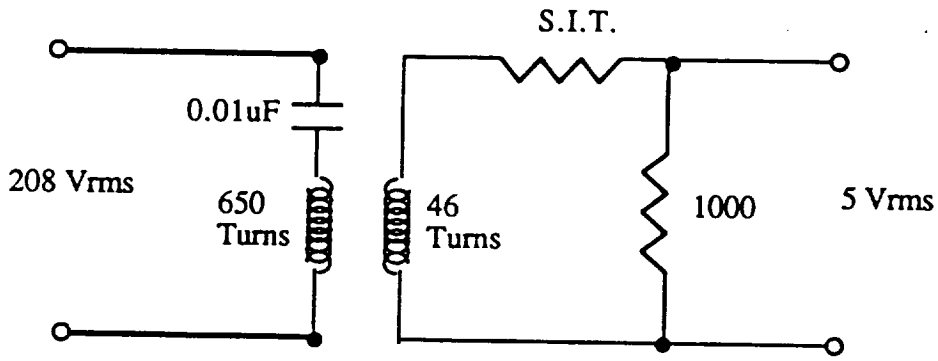

Figure 4.7.2-1 AC Voltage Sensor

4.8 AC Current Sensors

4.8.1 AC Current Sensor Requirements

An AC Current Sensor is required to provide a differential voltage input to one of 16 current sensor channels present on an A/D card. The output voltage of the current sensor for various current sensor values is listed in Table 4.8.1-1.

Frequency	Current Sensor Value Input	Reqd Output Voltage Level
20 kHz	50 mA Ground Fault	5.00 +/- 0.25 Vrms
20 kHz	15A	5.00 +/- 0.25 Vrms
20 kHz	50A	5.00 +/- 0.25 Vrms
20 kHz	100A	5.00 +/- 0.25 Vrms
20 kHz	125A	5.00 +/- 0.25 Vrms

Table 4.8.1-1 - AC Current Sensor Requirements

4.8.2 AC Current Sensor Design

The 15, 50, 100, and 125 AC Current sensors (Figure 4.8.2-1) are comprised of a 1:200 turn transformer with appropriate burden resistors to provide a 5 Vrms output at rated current.

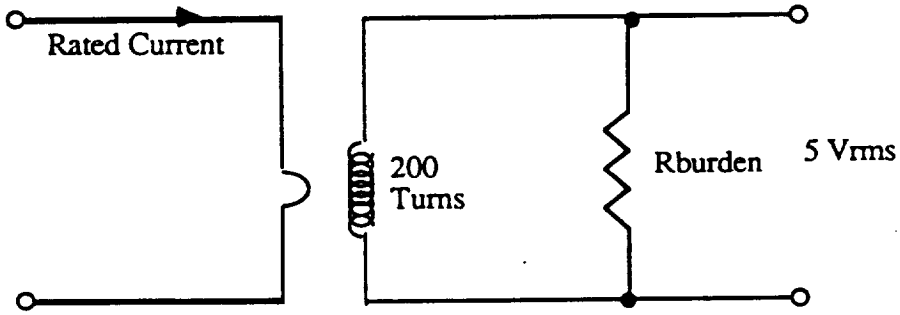

Figure 4.8.2-1 AC Current Sensor

The 50 mA differential AC Current sensor (Figure 4.8.2-2) is comprised of a 15 turn source and return primary winding and a 200 turn secondary winding. The sensor is designed to handle up to 10 kW at 208 Vrms, 20 kHz and to output 5 Vrms at 50 mA differential current between the source and return windings.

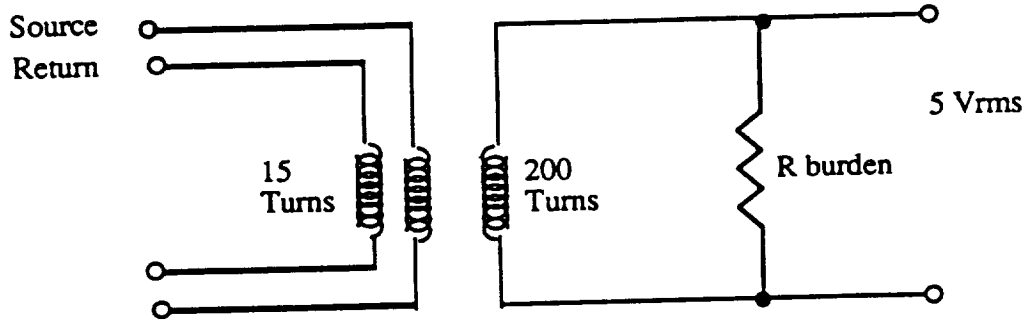

Figure 4.8.2-2 50 mA Current Sensor

4.9 Temperature Sensors

4.9.1 Temperature Sensor Requirements

A temperature sensor is required to provide a variable resistance input to one of the 16 temperature channel inputs on an A/D card. The output resistance of the temperature sensor for minimum and maximum temperatures is listed in Table 4.9.1-1.

Temperature (Celsius)	Temp. Sensor Resistance (Ohms)
-30	8806 +/- 500
+85	2342 +/- 500

Table 4.9.1-1 - Temperature Sensor Requirements

4.9.2 Temperature Sensor Design

The temperature sensors selected for use in the ACM/PMAD breadboard are LTN-11C (Linear Thermistor Network) sensors. The impedance of the output of the sensors is inversely temperature dependent. The sensors satisfy the requirements as listed in Table 4.9.1-1.

4.10 DC Remote Power Controller (RPC)

4.10.1 DC RPC Requirements

The DC Remote Power Controller is a single-pole, single-throw switch required to provide 8.33A (1 kW) or 25.0 A (3 kW) at 120 VDC to any resistive, capacitive, or inductive load. The switch is required to operate either above or below a load with the switching occurring via a solid state switch. Commanding on and off of the RPC is controlled by a GC Card.

The RPC provides the GC with analog current and temperature sensor data. Additional data which is passed to the GC includes a switch status indicator and an under voltage trip bit.

A current limiter control circuit is present on the DC RPC. The current limiter limits the current during a fault condition to 400% RMS during the first one microsecond of an event. The RPC will go into a current limit operation within one microsecond and limit the current to 175% RMS for a time constant which is dependent upon the voltage across the switch at the time. A dead short will result in the RPC turning off in approximately 15 mS.

4.10.2 DC RPC Design

The DC RPC (Figure 4.10.2-1) is designed to be a self-protecting, SPST switch controlled from a GC card. The main parts that comprise the RPC are the switch power electronics and the switch control circuitry.

The power handling components of the DC RPC include the current measuring shunt, the current limiting inductor, the MOSFET switches, and the current sense resistors.

Current enters the RPC via the shunt which provides analog current information to an isolation amplifier and subsequently to the GC card. This input is the input to the I^2t processor which resides on the GC card. A 1 μH inductor is in series with the main power path to limit di/dt

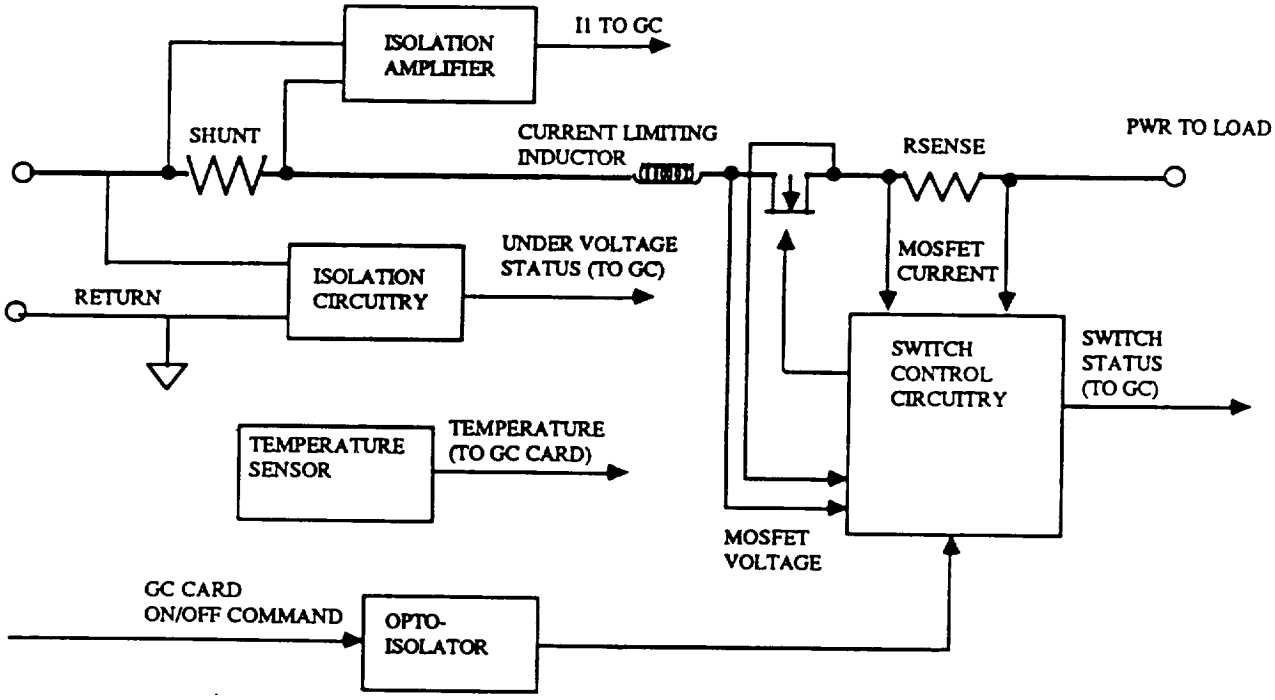

Figure 4.10.2-1 DC Remote Power Controller (RPC)

during a surge event prior to the current limiting control loop responding. Six MOSFET stages for the 1 kW DC RPC and 18 MOSFET stages for the 3 kW DC RPC are paralleled to handle the power and reduce the voltage drop across the switch. The sense resistors provide feedback to the switch control circuitry which provides overload protection to the RPC.

The switch control circuitry takes the GC card ON/OFF command line, the MOSFET current, and the MOSFET voltage and decides how to operate the switch. Any time an OFF command is issued from the GC card, the RPC is off. The only time the switch can be on is if the GC card has issued an ON command.

During non-overload conditions, the MOSFETS are saturated if an ON command has been issued. Any current fault which exceeds 175% rated value will cause the RPC to go into a current-

source mode of operation (the MOSFETs run linear). The voltage across the switch is sensed and integrated and compared to a reference signal. If a dead short exists on the output of the RPC for > 15 mS, the RPC will latch off. If the short is removed prior to 15 mS (in the case of charging a capacitor bank), the switch will turn back on and the MOSFETs will re-saturate.

Additionally, the DC RPC provides an under voltage signal to the GC card which allows it to trip off the RPC if the line voltage falls below 60 VDC. The RPC is capable of operating either in the positive or negative leg of the load. The DC RPC as presently implemented in the MSFC breadboard does not contain ground fault detectors due to the nature of the grounding configuration which was implemented in the system. The RPCs would need to be designed to wwitch both the positive and the return sides of the power in order to incorporate ground fault detection.

4.11 DC Remote Controlled Circuit Breaker (RCCB)

4.11.1 DC RCCB Requirements

A DC Remote Controlled Circuit Breaker is required to provide 83.3 A (10 kW) at 120 VDC to up to 3 fully-loaded 3 kW DC RPCs. The switch is SPST and consists of several parallel power MOSFETS which switch the positive side of the +120 Vdc. The RCCB may be switched "hot".

The RCCB is required to trip off on any current exceeding 300% for 150 mS. The RCCB will also trip off on any current exceeding 110% for 5 seconds. The RCCB returns switch status information to the GC card, as well as an analog current level signal.

The DC RCCB is required to dissipate <1% of power rating at full load, and have a voltage drop of <1.5 VDC. The DC RCCB is controlled and commanded on and off from a GC card.

4.11.2 DC RCCB Design

The DC RCCB (Figure 4.11.2-1) is a single-pole, single-throw solid-state switch comprised of a power stage unit developed by Teledyne Electronics and an interface electronics

unit. A copy of the Product Control Drawing (PCD) for the Teledyne power stage unit can be found in Appendix IV (Note: This unit is called an RPC in Appendix IV and is not to be confused with the Martin Marietta RPC).

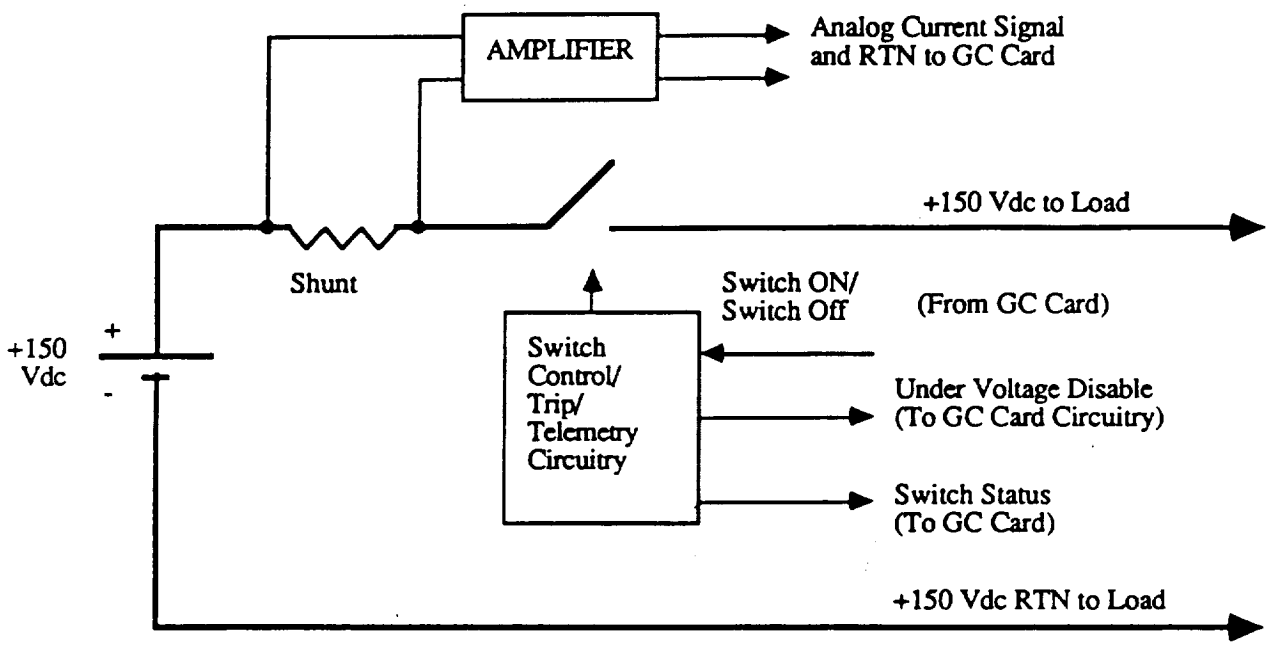

Figure 4.11.2-1 DC Remote Controlled Circuit Breaker (RCCB)

The power stage is comprised of a number of MOSFET switches in parallel capable of switching 120 VDC, 83.3A. The power stage has a built-in over current curve and is capable of tripping off during over current conditions. Additionally, the power stage has an under voltage lockout circuit which will turn the switch off if the line voltage falls below approximately 60 VDC. The RCCB needs to be commanded off and then on in order to reset the switch.

The interface electronics provide necessary switch status information and current telemetry information to the GC card. The current level feedback is from a 200 A shunt and amplifier. If the

current exceeds 110% of nominal, the GC card will issue an off command to the RCCB via an I2t trip condition.

4.12 DC Remote Bus Isolator (RBI)

4.12.1 DC RBI Requirements

A DC Remote Bus Isolator is required to provide 15 kW, 120 VDC to RCCB switches. The switch is SPST and consists of a large relay which switches both the positive and return sides of the DC power. The RBI can only be switched when the DC power is off.

The RBI provides the GC card with relay status information only. Commanding the RBI on and off is controlled by a GC card.

4.12.2 DC RBI Design

The DC RBI (Figure 4.12.2-1) is designed to provide DC power to a DC RCCB. The main parts that comprise the RBI are the relay and the relay interface electronics.

The relay is used as a single pole, double throw magnetically latching relay with 2 power contacts and an auxiliary contact used for relay status information. The relay is manufactured by Leach Corp., and has a current rating of 120 amps. The RBI cannot be switched hot.

The relay interface electronics included protection diodes across the relay coils, an inductive kickback prevention diode for the +15 VDC supply from the GC Card, and an energy storage capacitor to insure rapid turn on and turn off of the relay.

4.13 DC Voltage Sensor

4.13.1 DC Voltage Sensor Requi ements

A DC voltage sensor is required to provide a differential isolated voltage input to one of 16 voltage channels present on an A/D card. The secondary voltage is required to be 5.00 +/- 0.25 Vrms for a primary input of 120 VDC.

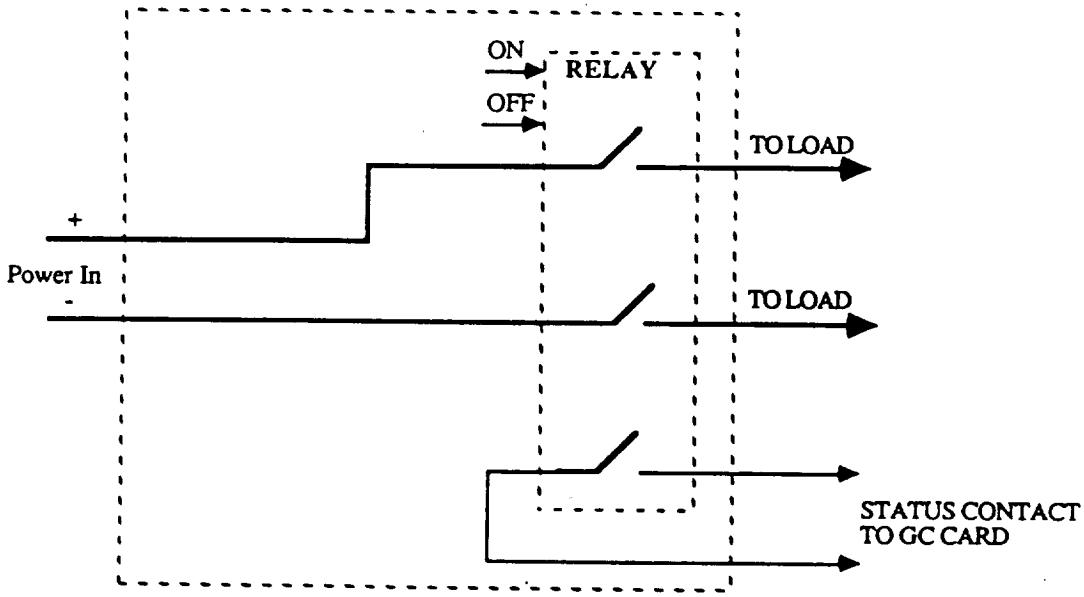

Figure 4.12.2-1 AC/DC Remote Bus Isolator (RBI)

4.13.2 DC Voltage Sensor Design

The DC voltage sensor (Figure 4.13.2-1) is comprised of a resistor-divider network which inputs to an AD 289J isolation amplifier. The resistor-divider provides a sufficient attenuation of the 120 VDC allowing for an analog signal to be input to the isolation amplifier. A zero-offset and an adjustable gain potentiometer are present which allows the output of the isolation amplifier to be set at 0 VDC for 0 VDC input and at 5 VDC for 120 VDC input.

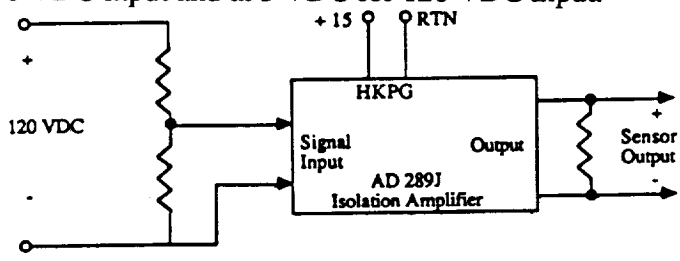

Figure 4.13.2-1 DC Voltage Sensor

4.14 DC Current Sensors

4.14.1 DC Current Sensor Requirements

A DC Current Sensor is required to provide a differential voltage input to one of 16 current sensor channels present on an A/D card. The output voltage of the current sensor for various current sensor values is listed in Table 4.14.1-1.

Frequency	Current Sensor Value Input	Reqd Output Voltage Level
DC	15A	5.00 +/- 0.25 VDC
DC	50A	5.00 +/- 0.25 VDC
DC	100A	5.00 +/- 0.25 VDC

Table 4.14.1-1 DC Current Sensor Requirements

4.14.2 DC Current Sensor Design

The DC current sensor (Figure 4.14.2-1) is comprised of a current shunt which inputs an analog signal to an AD 289J isolation amplifier. A zero-offset and an adjustable gain potentiometer are present which allows the output of the isolation amplifier to be set at 0 VDC for 0 amps input and at 5 VDC for rated current input. An external 15 VDC supply is required to power the isolation amplifier.

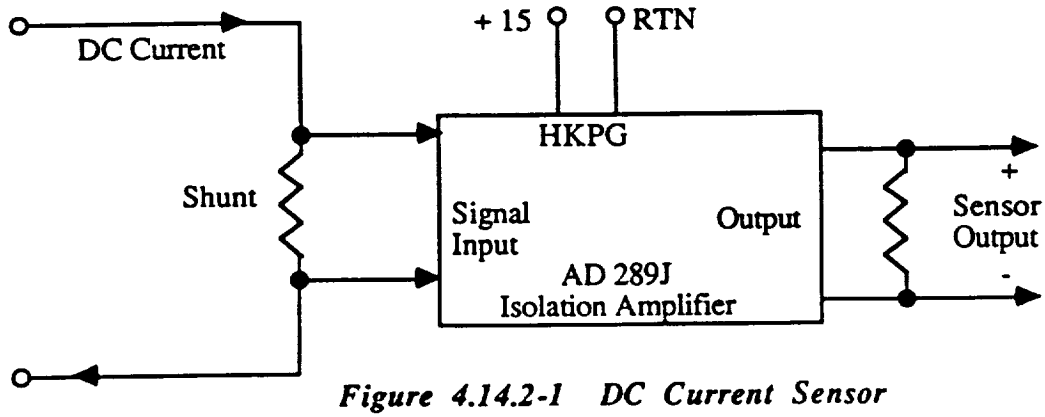

Figure 4.14.2-1 DC Current Sensor

4.15 Card Cage

A card cage is required to provide slot mounting and interface connectors for SIC, A/D, and GC cards. Each card cage is required to contain (2) sets of the hardware listed in Table 4.15-1. A detailed design drawing and description of the card cage can be found in Figure 4.15-1.

(2) SICs with LLP Cabling Interface
(1) A/D Card with Voltage, Current, and Temperature Sensor Connector Interfaces
(9) GC Circuits with Switch Connector Interfaces

Table 4.15-1 Card Cage Hardware Requirements

4.16 Test Tool

A test tool is required to provide easy access debugging capabilities for SIC, A/D, and GC cards. The test tool can simulate an RBI, RCCB, or RPC switch and corresponding switch status, fault, and command information. External control of the test tool can be accomplished using an LLP and manual mode software.

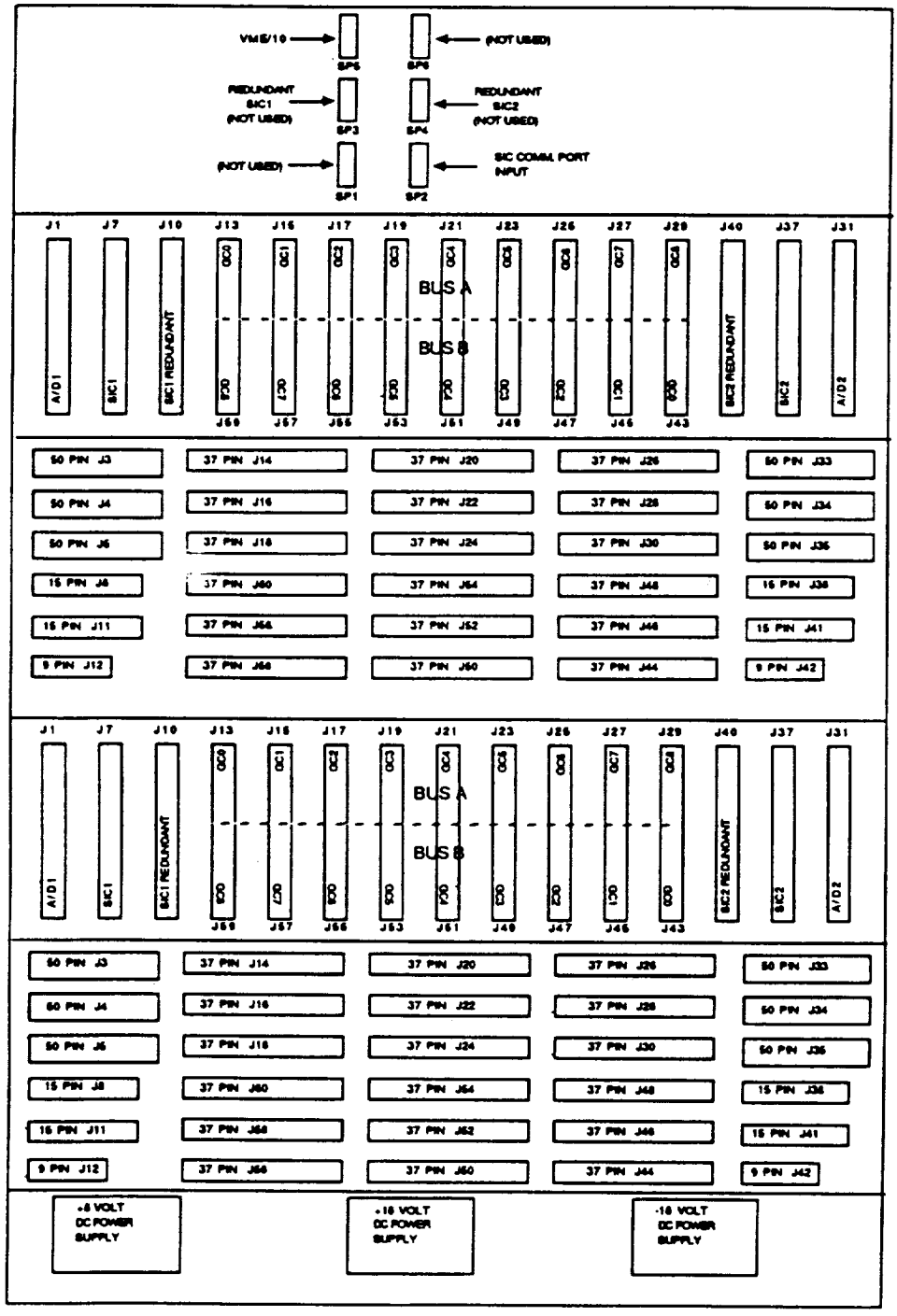

Figure 4.15-1 Card Cage

5.0 TASK IV

Common Module Power Management and Distribution Breadboard Testing

5.1 Switchgear Interface Controller (SIC)

The SIC cards have been integrated into the SSM/PMAD breadboard and have been tested with both the 20 kHz and the DC systems. The original design was modified to include optically isolated transmit and receive lines between the LLP and SIC to prevent the propagation of noise between the SIC and its LLP. One failure did occur during May of 1990 on a number of SIC cards when +120 VDC was inadvertently placed on the SIC card return (card cage signal return). The failure which occurred on the SIC cards would have been prevented if the opto-isolator boards would have been installed in the Lowest-Level Processors. This event resulted in the failure of a number of chips on the SIC including the line driver/receiver chip and a number of the RAM chips. The opto-isolator boards have since been installed in all of the LLPs to prevent the repeat of such an event. The LLP to SIC interface document (Appendix II) was completely tested with no discrepancies found in the design or operation of the SIC. Each SIC card has been tested with an LLP, 9 GC cards, and an A/D card attached.

5.2 Generic Controller (GC) Card

5.2-1 Generic Controller (GC) Card (Original)

The original GC cards have successfully been integrated into both the 20 kHz and DC MSFC breadboards with no known major problems to date. All noise-related design problems were diagnosed and fixed during development testing of the 20 kHz system in Denver and at MSFC. These problems included receiving an inadvertent under voltage trip during a faulted event and an inadvertent over current trip during a turn on. The inadvertent under voltage trip problem was fixed by adding additional capacitance to the input of the under voltage trip processor on the GC card. The inadvertent over current trip was remedied by adding a small filter capacitor to the output of the over current trip analog comparator. Both of these problems were due to the high impedance characteristics of the 20 kHz source and cabling.

One system level operation problem occurred during a software buy-off at MSFC when the +10 VDC unregulated housekeeping supply feeding the system was over loaded. This over loading of the housekeeping supply caused the supply to go into a current supply mode of operation. The housekeeping voltage dropped substantially causing the linear regulators on the GC card to drop out of regulation. Once the GC housekeeping voltage dropped out, the ALTERA chip no longer functioned correctly. This caused a series of switches to turn on and off seemingly at random. This problem was fixed by inserting a +10 VDC supply into the system that had more current capability than the original supply.

5.2-1 Generic Controller (GC) Card (DC-Only Design)

The DC-only GC cards have successfully been integrated into the DC MSFC breadboard with no known problems to date. This new design alleviates much of the complexity which resides within the original GC card design.

5.3 Analog to Digital (A/D) Card

The A/D cards integrated into the MSFC breadboard with no known problems. All sensor readings have been accurate and consistent when the sensors are properly installed. One issue that has been brought to attention has been the lack of resolution which the sensor readings experience due to the fact that the A/D card has only 8 data bits (it returns 7 bits of data). When a sensor is reading low on its scale (say, 2 amps on a 50 amp sensor), the precision error due to the 7 bit conversion can cause a substantial inaccuracy in reading the actual value. The solution to this problem would be to use a higher-resolution A/D board in the system (say, 12 bits).

5.4 AC Remote Power Controller RPC

The AC remote power controllers were successfully integrated in the 20 kHz MSFC breadboard. One major problem which occurred during integration was an inadvertent Solid State ON/ Mechanical Off condition on the RPC. This condition was caused by EMI noise being

injected into the fast trip over load protection circuitry on the RPCs during a transient event in the system. This problem was corrected by inserting filter capacitors and resistors in strategic locations in the fast trip circuitry. Additionally, EMI chokes and RC snubbers were added in strategic locations on the 20 kHz power lines to minimize EMI generation.

Figure 5.4-1 shows a fast trip (dead short) event on the AC RPC. This feature of the RPC was tested many times during hardware integration at MSFC.

5.5 AC Remote Controlled Circuit Breaker (RCCB)

The AC remote controlled circuit breakers have been successfully integrated into the MSFC breadboard. The maximum 20 kHz power which has been routed through the RCCBs has been 5 kW to date due to source limitations.

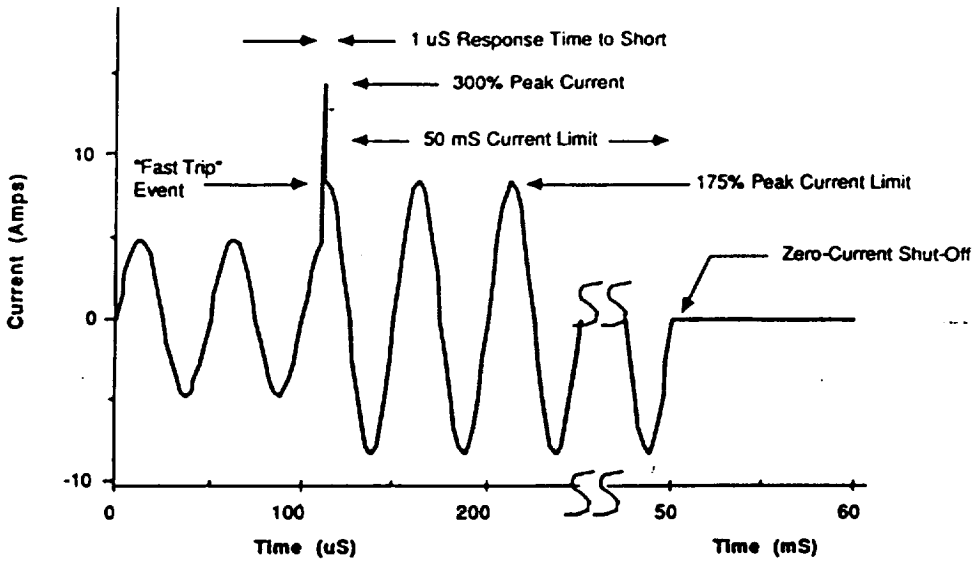

Figure 5.4-1 AC RPC Fast Trip Event

5.6 AC Remote Bus Isolator (RBI)

The AC remote bus isolators have been successfully integrated into the MSFC breadboard. The maximum 20 kHz power which has been routed through the RBIs has been 5 kW to date due to source limitations.

5.7 AC Voltage Sensors

The AC voltage Sensors have been successfully integrated into the MSFC breadboard. Careful consideration was taken in routing wires from the output of the sensor to the input of the A/D card. Twisted pair wires were run between the sensor output and the A/D input which minimized noise pickup and generation.

5.8 AC Current Sensors

The AC Current Sensors have been successfully integrated into the MSFC breadboard. Careful consideration was taken in routing wires from the output of the sensor to the input of the A/D card. Twisted pair wires were run between the sensor output and the A/D input which minimized noise pickup and generation.

5.9 Temperature Sensors

Temperature sensors have not been integrated into the MSFC breadboard to date. The temperature channels on the A/D card have been thoroughly tested with temperature sensor simulator resistors to fully verify this feature. At a future date, temperature sensors can be easily installed into the MSFC breadboard. Proper mounting techniques and twisted pair wires should be used in their installation.

5.10 DC Remote Power Controller (RPC)

The DC remote power controllers have successfully been integrated into the DC MSFC breadboard. One minor mechanical problem occurred during the integration of the boards with the system. Two DC RPC boards experienced mechanical failure of UES 706 stud-mounted diodes during mechanical installation of the boards into the system. These broken diodes caused input to output shorting of the RPCs. The UES 706 diodes were replaced on these RPCs which eliminated the problem. The DC RPCs as existing in the present breadboard configuration do not provide ground fault protection because the RPC was designed to only switch the "hot side" current. If ground fault protection were to be implemented, it would be necessary to design the system so the RPC switched both the hot and the return sides of the power.

Figure 5.4-1 shows a fast trip (dead short) event on the DC RPC. This feature of the RPC has been tested many times during hardware integration at MSFC.

5.11 DC Remote Controlled Circuit Breaker (RCCB)

Design, development, and acceptance testing of the DC RCCBs has occurred at MMAG in Denver. Cooling fans need to be installed for the DC RCCBs when running above 5 kW power. The current over load trip on the DC RCCB is approximately 102% of nominal - slightly below the 115% level specified in the Task III discussion of the RCCB. This discrepancy is do to the fact that the input voltage specification was changed from 150 VDC to 120 VDC midway during development of the units. The particular current trip circuitry present on the Teledyne unit is difficult and impractical to change. Integration of the DC RCCBs has not occurred at MSFC due to a bus configuration change.

5.12 DC Remote Bus Isolator (RBI)

The DC remote bus isolators have been successfully integrated into the MSFC breadboard. No known problems have existed to date with the DC RBIs.

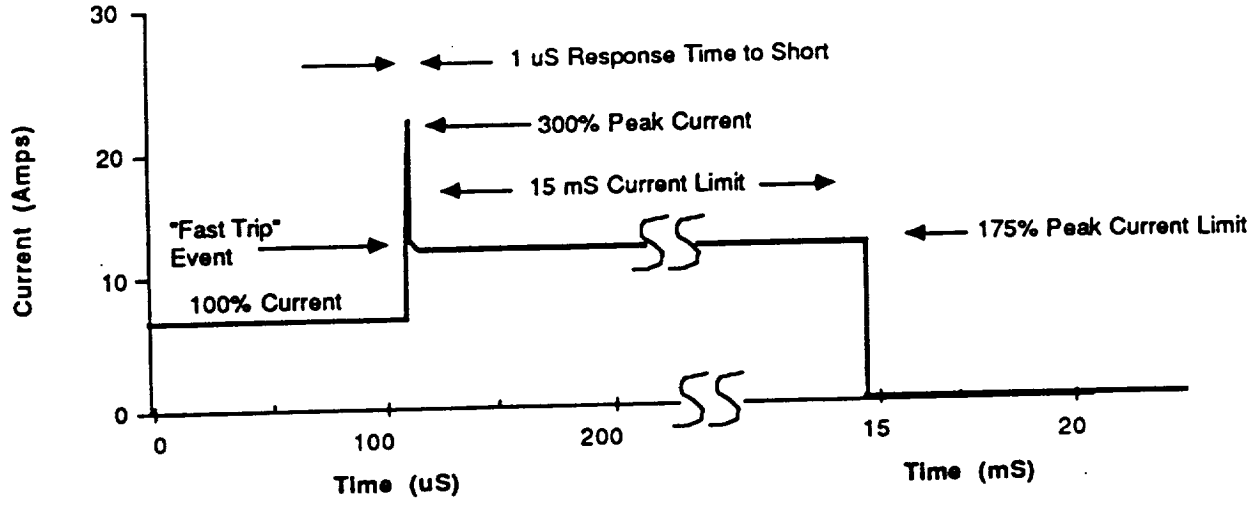

Figure 5.10-1 DC RPC Fast Trip

5.13 DC Voltage Sensors

The DC voltage Sensors have been successfully integrated into the DC MSFC breadboard. Careful consideration was taken in routing wires from the output of the sensor to the input of the A/D card. Twisted pair wires were run between the sensor output and the A/D input which minimized noise pickup and generation. A +15 VDC external power supply is required for the AD289J isolation amplifier housekeeping. Careful consideration was made as to how the wires were routed from the power supply to the sensor and from the output of the sensor to the input of the A/D card. Twisted pair wires were run between these points which minimized noise pickup and generation.

5.14 DC Current Sensors

The DC Current Sensors have been successfully integrated into the DC MSFC breadboard. Careful consideration was taken in routing wires from the output of the sensor to the input of the

A/D card. Twisted pair wires were run between the sensor output and the A/D input which minimized noise pickup and generation. A +15 VDC external power supply is required for the AD289J isolation amplifier housekeeping. Careful consideration was made as to how the wires were routed from the power supply to the sensor and from the output of the sensor to the input of the A/D card. Twisted pair wires were run between these points which minimized noise pickup and generation.

5.15 Card Cage

The card cages have been integrated into the MSFC breadboard with no known problems to date. It is very important that the unregulated +10, +20, and -20 VDC supplies that provide housekeeping power to the cards in the card cage have sufficient current output capability to drive the system. The problem that occurred during software buy-off was the result of the +10 VDC housekeeping supply being over loaded.

5.16 Load Converter

The task of designing and developing a DC - 400 Hz load converter was cancelled and the efforts re-directed. This task included designing, fabricating, and testing of a DC to AC inverter box. The criteria listed in Table 5.16-1 were the established functional/performance goals.

Three separate load converter designs were anaylzed as possible topologies for the MSFC breadboard unit. A list of these topologies and a brief discussion of each is included in Table 5.16-2. The switch-mode power amplifier PWM converter was the selected topology. A down-scaled version of this converter was breadboarded and a test report prepared which is located in Appendix V of this final report.

Table 5.16-1 Load Converter Design Goals

Inverter Output

Voltage - MIL-STD-704D Three-Phase 400 Hz 120V rms Line to Neutral.
Current - 4.0 Amperes rms maximum per phase.
Power Factor - 0.9 leading to 0.7 lagging.
Power - 175W nominal to 480W maximum per phase.

Inverter Input

Voltage - 90.0 VDC minimum to 150 VDC maximum.
Current - Not to exceed 15.0 ADC steady state.
EMI - Per MIL-STD-461C Notice 3

General

Ground Currents - Less than 5.0 mA rms in ground interconnect wire shorting all output grounds to input return.

Table 5.16-2 Load Converter Technologies

Resonant-Link Cyclo Converter: This topology utilizes series resonant inverter technology mixed with pulse density modulation. High frequency SRI power is pulse density modulated to create low frequency regulated power.

Tri-Phase MAPHAM Converter: This topology utilizes a previously developed MMC SRI technology known as the MAPHAM Converter. This application as a DC - 400 Hz three-phase load converter requires some redesign since the original MAPHAM which was built and tested was a single phase 20 kHz converter.

Switched-Mode Power Amplifier: This approach employs DC to DC converter principles such as pulse width modulation using a sinusoidal instead of a DC reference.

APPENDIX I

Switchgear Technology Assessment

1. Introduction

The objective of this task is to identify pieces of equipment which require development efforts to support the Space Station phase C/D effort. The approach to this task is shown in Figure I.1-1. Equipment lists were developed from the previously selected network schematics to define the basic functional requirements for network equipment. In addition, other requirements which affect the suitability of specific items for use on the Space Station program have also been identified. Although program ancillary requirements such as outgassing do not affect the state of the art in switchgear technology, they can provide the basis for rejecting an otherwise acceptable item, and are therefore included in this assessment.

An industry survey was performed to identify existing sources for components such as switchgear, sensors, fuses, and transient suppressors. In addition, a survey of recent research and development in the area was performed to identify near term sources of equipment. The data obtained in these surveys is documented in an equipment database.

Upon the completion of the surveys and requirement definition, the equipment database was correlated with the equipment lists to determine the existence of ready equipment, not needed equipment, and equipment requiring development. The data was then screened with respect to the ancillary requirements, and then finally categorized for technology readiness.

2.0 Technology Levels

The technology levels defined for the purposes of this study are ready, near ready I, near ready II, and not ready. Technology ready is defined as a part which may be ordered and flown with no modification. Near ready type I is defined as an existing part which could be flown with only minor modifications. An example of this is a relay which was designed for use in aircraft which is functionally suitable for use, but does not meet program materials requirements for

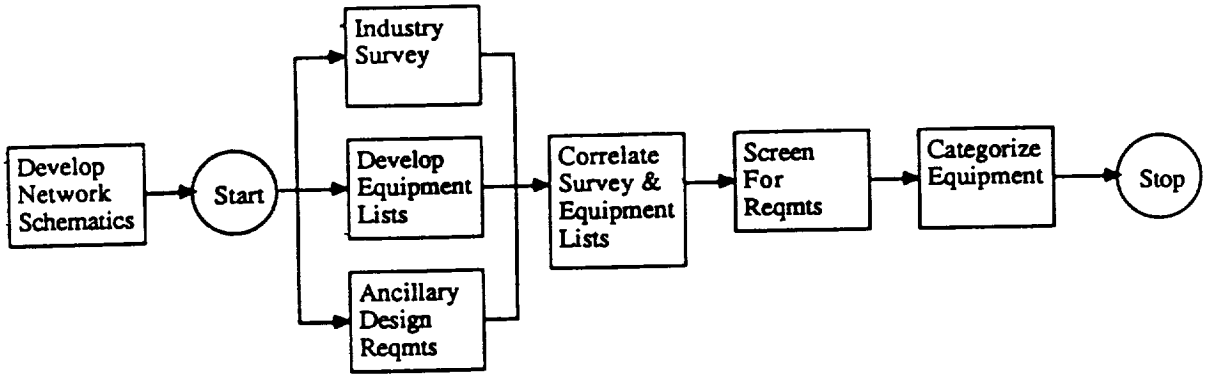

Figure I.1-1 Switchgear Technology Assessment

vacuum stability. Near ready type II is defined as a part requiring significant development effort to meet the functional and ancillary design requirements for space station use, but which can be developed within the constraints of the space station advanced development activity. Technology not ready equipment is defined as requiring development beyond the constraints of the space station advanced development activity. Equipment not required is defined as an item which is not desirable in the system due to incompatibility with the design approach taken.

3.0 Definition of Terms

This technology addresses all equipment required to implement the network topologies selected for development. We have found in our industry survey that nomenclatures are inconsistent relative to the functions and characteristics of given devices. To avoid confusion in this document we will define specific nomenclatures for specific characteristics. A Remote Power Controller (RPC) is a solid state switch / circuit breaker which limits current during overload conditions prior to tripping. A solid state breaker (SSB) is an equivalent device except that no current limiting is provided, and trip times are typically shorter. A remote control circuit breaker (RCCB) is an electro-mechanical device with remote control on / off / reset capability. A remote

bus isolator is a device used for re-configuring the distribution network, which has no current interrupt capability.

4.0 Design Approach

The equipment selected to implement a given network topology is driven by several considerations. The first consideration in the selection of switchgear and circuit protection devices is source impedance. Available fault current is driven largely by source impedance. Power sources which store a great deal of energy such as generators driven by solar dynamic collection systems and batteries are capable of delivering fault currents an order of magnitude greater than rated capacity. Conversely, inverters with current limited outputs will deliver currents on the order of two to three times rated output. Circuit protection devices much be sized to interrupt the worst case fault current which is strongly influenced by source impedance. The approach taken in developing RCCBs to provide this interrupt capability is to either significantly upgrade the device contacts, or to provide an additional pair to assist in the interrupt. In extreme cases where the breaker contacts would be prohibitively large, fuses are added in series with the breaker to provide the interrupt capability needed for a worst-case fault. An alternative approach is to provide current limiting capability with an RPC. This can be implemented using one of two methods - either an inductor can be switched into the circuit, or the RPC can provide foldback capability. Series inductance is an attractive approach for AC RPCs because it results in significantly less part stress on the switch than does foldback. Power dissipation during fault interrupts is reduced and thermal design of the device is greatly simplified using this approach. In DC systems, foldback is more attractive because the size of the inductor is a linear function of the time that the current must remain below a given level prior to the RPC trip.

Level in the distribution network is also a consideration in the selection of switchgear. At the load level of the distribution network, current limiting is highly desirable because the available fault current is higher than the current at which the wiring will fuse. Inrush limiting and motor soft start capability are needed. Current limiting also prevents a faulted load from affecting other loads connected to the bus. Secondary distribution switchgear may be either an RPC or an RCCB. The advantages of RCCBs are lower voltage drop and decreased thermal dissipation. RPCs save copper weight by limiting fault current, and will prevent a faulted rack from affecting other racks.

A consideration in providing current limiting at the secondary and primary distribution levels is the possibility of causing brown out conditions at the lower levels during overloads and fault conditions. This is because the impedance added to limit over currents also softens the source. As the RPC goes into the current limit mode, the output voltage will fall considerably. This continues for the entire trip time of the RPC which is in the tens of milliseconds region. Conversely, a breaker and fuse would provide the available fault current for a short period and then open, thereby eliminating the long term bus under voltage.

Coordination of protection is also a consideration in the selection of a switchgear type. The term coordination refers to a system where a given branch in the distribution network is protected by the device immediately above it. Devices higher in the network must be sized for larger currents than the devices down stream. This concept also limits the use of current limiting devices in the higher levels of a distribution network. An RPC in the primary distribution level of a network with RCCBs located in the secondary level could result in a fault condition on the secondary where the current limited primary would not deliver enough current to open the breaker prior to the RPC trip. In networks where two levels are current limited, the higher level current limit must be high enough that a fault on the lower level does not drive the upper level into the current limit mode.

The selected approach to the common module power management and distribution system is to provide current limiting RPCs at the load center level, RCCBs at the secondary distribution assembly, and RCCBs at the primary distribution assembly base on the previously discussed considerations. RPCs will also be carried as an option at the secondary distribution assembly for the final technology assessment. Ground fault protection will be provided on power leads to which the crew has access. Instrumentation required to implement the autonomy approach selected in the ACM/PMAD contract is also included.

5.0 Equipment List

The equipment lists in Table I.5-1 describes the hardware required to implement the selected network topologies.

Table I.5-1 Network Topology Hardware

POWER DISTRIBUTION EQUIPMENT LIST (REV. 1)

LOCATION	MEASUREMENT EQUIPMENT LISTING			SWITCH GEAR	
PPDA PRIMARY POWER DISTRIBUTION ASSEMBLY	AC: (400 Hz) THREE PHASE			RCCB	
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	115Vac	150Vac		
	Current*	100A	100A	100A/Phase 3PST	
	Transient Suppressor	200A	200A	200A/Phase 3PST	
	Temperature Sensor				
	Fuses	100A			
		200A			
	DC:				
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	150Vdc	200Vdc		
	Current*	200A	200A	200A SPST	
	Transient Suppressor	350A	350A	350A SPST	
	Temperature Sensor				
	Fuses	200A			
		350A			
SDA SECONDARY DISTIBUTION ASSEMBLY	AC: (400 Hz) THREE PHASE			RPC	RCCB (Opt)
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	115Vac	150Vac		
	Current*	10A	10A	10A/Phase 3PST	10A/Phase 3PST
	Transient Suppressor	50A	50A	50A/Phase 3PST	50A/Phase 3PST
	Temperature Sensor				
	Fuses	10A			
		50A			
	DC:				
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	150Vdc	200Vdc		
	Current*	20A	20A	20A SPST	20A SPST
	Transient Suppressor	100A	100A	100A SPST	100A SPST
	Temperature Sensor				
	Fuses	20A			
		100A			
LC LOAD CENTER	AC: (400 Hz) THREE PHASE			RPC	RBI
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	115Vac	150Vac		
	Current*	3A	3A	3A/Phase 3PST	10A/Phase 4PST
	Transient Suppressor				
	Temperature Sensor				
	** Ground Fault Detector				
	DC:				
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	150Vdc	200Vdc		
	Current*	10A	10A	10A SPST	20A 2PST
	Transient Suppressor				
	Temperature Sensor				
	** Ground Fault Detector				

* Switch Gear may provide Current Monitors

** Switch Gear may provide Ground Fault Detection

NOTE: Current monitors are capable of overranging

Table I.5-1 Network Topology Hardware (Concl)

POWER DISTRIBUTION EQUIPMENT LIST(CONT)

LOCATION	MEASUREMENT EQUIPMENT LISTING			SWITCH GEAR	
	AC: (400 Hz) THREE PHASE			RPC	RBI
NDA NODE DISTRIBUTION ASSEMBLY	TYPE	MAGNITUDE	MONITOR RANGE	(RCCB Opt)	
	Voltage	115Vac	150Vac		
	Current*	20A 100A	20A 100A	20A/Phase 3PST	100A/Phase 4PST
	Transient Suppressor				
	Temperature Sensor				
	Fuses	20A			
	DC:				
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	150Vdc	200Vdc		
	Current*	35A 200A	35A 200A	35A SPST	200A 2PST
	Transient Suppressor				
	Temperature Sensor				
	Fuses	35A			
NLC NODE LOAD CENTER	AC: (400 Hz) THREE PHASE			RPC	
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	115Vac	150Vac		
	Current*	3A	3A	3A/Phase 3PST	
	Transient Suppressor				
	Temperature Sensor				
	DC:				
	TYPE	MAGNITUDE	MONITOR RANGE		
	Voltage	150Vdc	200Vdc		
	Current*	10A	10A	10A SPST	
	Transient Suppressor				
	Temperature Sensor				

* Switch Gear may provide Current Monitors

NOTE: Current monitors are capable of overranging

6.0 Industry Survey

The results of the industry survey are documented in the electrical system component data base. Sources of RPCs, RCCBs, RBIs, SCCBs, current sensors, voltage sensors, temperature sensors, fuses, and transient suppressors have been identified. In addition to industry sources, research and development by government has been included. There sources are listed in Table I.6-1.

Source	Component(s)
Westinghouse	RPC, RBI, SCCB
Leach	RPC, RBI, RCCB
Eaton (Cutler Hammer)	RCCB, RBI
LeRC	RPC, RBI
Hartman Relay	RBI, RCCB
Teledyne	RPC, SSCB
Bussman	Fuses
Honeywell	Sensors
General Semiconductor	Transient Suppressors
RCA	Transient Suppressors
AET	Sensors
OSI	Sensors
Tracor	Fuses

Table I.6-1 Industry Survey Component Data Base

The database has the capability to sort records by device type, functional characteristics, manufacturer, and part number. Output from the database will be included in the final technology assessment.

7.0 Design Requirements

The space station ancillary design requirements which affect the suitability of components for program use are listed below in Table I.7-1.

Document Number	Title
NHB 1700.7A	Safety Policy and Requirements for STS Payloads
NHB 8060.1B	Flammability, Odor, and Offgassing Requirements and Test Procedures for Materials in Environments that Support Combustion.
NASA TM 86498	Natural Environment Design Criteria for the Space Station
JSC 16888	STS Microbial Contamination Control Plan
MSFC STD 506B	Standard Materials Process Control
SP-R-0022A	General Specification, Vacuum Stability of Polymeric Materials for Spacecraft Application
MSFC-SPEC-250	Material Corrosion
MSFC-HDBK-527D	Materials Selected List for Space Hardware Systems

Table I.7-1 Space Station Ancillary Design Requirements

8.0 Technology Assessment

8.1 Remote Power Controllers

We have identified several possible sources of flight type RPCs. Leach has developed a single phase 115 V, 400 Hz device which utilizes a series inductance to limit current during power up and faults. A three phase unit is also under development and scheduled to be complete later this year. The Leach RPC uses MOSFETS to implement the power switch. MOSFETs are the most preferred devices for use in RPCs because they are easily paralleled to reduce voltage drop and flight qualified parts are available.

Teledyne also has the capability to produce flight type RPCs. The Teledyne approach to developing RPCs is to adapt existing hybrid switching and control circuits to implement desired functions. The Teledyne RPC utilizes a foldback technique to limit current. A 115 V, 400 Hz unit is available and in use on the F-16.

Westinghouse has built a flight-qualified single-phase 115 V, 400 Hz, 1.5 Amp unit for use on the original B-1 program. When the program was cancelled, the RPC had already completed qualification testing. The Westinghouse RPC utilizes MOSFETs for the power switch, and foldback current limiting. Although the RPC is not available as part of the Westinghouse standard product line, the capability to produce a flight unit exists.

In general, the state of the art in RPCs is in the near ready category. Qualified aircraft type units exist and could be modified for use in the space station. Leach is actively involved in developing space type RPCs, and their approach does have several advantages. The practical limit in the size of an RPC that can be built is the number of devices which can be successfully paralleled on a hybrid. The number of devices required to implement a given size RPC is a function of the allowable on-state power dissipation, and part stress during current limiting. The Leach approach minimizes part stress during fault interrupt, and may allow a larger device to be built. The existing unit is rated at ten amps. This technology is easily extended to three phases. We believe that a practical limit in RPC design in twenty amps. This would yield a three-phase

unit rated at approximately seven KVA. An appropriately de-rated unit would than be in the 3 - 5 KVA range.

8.2 Remote Control Circuit Breakers

Three sources of RCCBs exist today. Cutler Hammer Builds aircraft-type units which will interrput up to 1000% of the rated current of the device. This is achieved by employing two pairs of contacts; a pair made of tungsten to tolerated arcing, and a pair made from precious metal to carry the current when the contacts are closed.

Leach also builds RCCBs. However, the high current interrupt capability is not provided on their existing units. This could be changed by using a larger contactor with a weight and volume penalty.

Hartman Relay will provide a custom hybrid to convert their standard contactor to a RCCB. This is not part of their normal product line, and the contactor must be sized for the worst-case interrupt.

The typical approach to building RCCBs is to build a control hybrid to open a power contactor when an over current is detected. Two issues associated with the use of RCCBs in power distribution networks are interrupt capability with stiff sources and actuation times when a hard short is encountered. An analysis will be performed as a part of the final assessment to resolve the issue of interrupt capability. This may not be a problem if the space station primary bus is driven by an inverter with a current limited output. The impact of actuation time is degraded power quality, and we will assess whether the results are acceptable. The general state of the art in RCCBs is in the near ready I category. Functionally acceptable units exist for aircraft which could be modified for space station use with minimal effort.

8.3 Solid State Circuit Breakers

Teledyne and Westinghouse have the capability to build SSCBs. The typical AC SSCB uses SCRs as the power switch , although DC units may use BJTs, MOSFETs, or GTOs.

We have categorized the SSCB as not needed because they perform the same functions as RCCBs except that the voltage drop is higher and the current is switched at zero in the AC units. Given that a short circuit has occurred, the zero cross switch is of limited benefit, because an abnormal condition has already been induced.

8.4 Remote Bus Isolator

A number of sources for RBIs have been identified. Since RBIs are not required to interrupt current, the development required to produce them is greatly reduced. Power contactors can be used to implement the function. We have developed a standard switchgear interface concept. RBIs are near-ready I because development is needed to implement the new interface. One issue associated with RBIs is arcing in high voltage DC applications. Hartman Relay has developed a technique for quenching arcs magnetically. We believe that their approach is adequate because we have tested one of their 270 VDC, 50 amp units and it passed life cycle testing. In addition, the U.S. Navy is actively involved in the development of high voltage DC switchgear for use in advanced aircraft designs.

8.5 Transient Suppressors

We have identified two sources of qualified transient suppressors. General Semiconductor manufactures a transorb which is qualified to Mil-S-19500 that can absorb 15 kW at peak power for one millisecond. This device was designed to be compatible with Mil-Std-704 type power systems. RCA is also a source of these devices. Transient suppressors are in the technology ready category.

Revision E of this Interface Control Document reflects the changeover to the new Intel based LLPs. Since Motorola and Intel store 16 Bit words in memory differently, this Interface Control Document had to be revised to reflect the difference. Anywhere the Switchgear Interface Card returned a 16 Bit word, the ICD has been changed to show the reversal of the high and low bytes. The only other change from revision D is the 1kW/3kW determination for DC RPCs in a standard switchword.

The following are SIC (Switchgear Interface Card) to LLP (Lowest Level Processor) commands, formats, and expected responses. The COMMANDS are messages from the LLP to the SIC. The RESPONSE is the actual data returned from the SIC in response to a command. The LLP will wait for a RESPONSE from the SIC after each command is sent. If no RESPONSE is received within 2 seconds, the SIC card will be considered nonfunctional. All COMMANDS sent to the SIC card will end with a CR (Carriage Return) which flags end of transmission to the firmware on the MVME331 card (intelligent communications controller). All RESPONSES from the SIC will also end with a CR for the same reason. The MVME331 card removes the CR before transmission from the SIC to LLP and from the LLP to the SIC.

NOTES:

The dip switch configuration for SIC is as follows:

Switch 1 - switch open (off) - bit0 high
Switch 2 - switch open (off) - bit1 high
Switch 3 - switch open (off) - bit2 high
Switch 4 - switch open (off) - bit3 high

The SIC port configuration is as follows:

Baud rate - 9600
Data bits - 8
Stop bits - 1
Parity - even

Status Format:

```
**************************************************************
 *    byte1    *       byte2      *       byte3      *    byte4    *
**************************************************************
```

where: byte1 -> $30 -- status OK
-> $31 -- status NOT OK

byte2 -> cc -- copy of command received
with MSB bit always set to 1

byte3 -> $80 -- status OK
-> $FF -- unknown command
-> $81 -- first byte not a command byte
-> $82 -- did not receive first data byte
-> $83 -- first data byte msb not high
-> $84 -- did not receive second data byte
-> $85 -- second data byte msb not high
-> $86 -- switch already on
-> $87 -- switch already tripped when
tried to turn it on
-> $88 -- switch already off
-> $89 -- switch already tripped when
tried to turn it off
-> $8A -- GC Data Valid error when
getting switch data

NOTE: If the following statuses are received, do not 'download' switch settings

-> $8B -- continous buffer overflow
(reset continous buffer)
-> $8C -- once buffer overflow
(redo once buffer)

NOTE: If the following statuses are received, the SIC card must be reset or must use the redundant SIC

-> $A1 -- SIC character buffer overrun
-> $A2 -- character overwritten (OE)
-> $A4 -- parity error from UART (PE)
-> $A6 -- OE and PE
-> $A8 -- framing error (FE)
-> $AA -- FE and OE
-> $AC -- FE and PE
-> $AE -- FE and OE and PE
-> $F7 -- SIC internal memory parity error

byte4-> $0D -- end of status

Command Word Format:

byte1	byte2	byte3	byte4

where: byte1 -> cc -- command
byte2 -> dd1 -- first byte of data word
byte3 -> dd2 -- second byte of data word
byte4 -> $0D -- end of command

Switchword Format:

	bit6=0 (switch not tripped)	bit6=1 (tripped)
bit0	current overrange H (1)	tripped overtemp latched H
bit1	S2 solid state swtch on H	S2 solid state swtch on H
bit2	S1 mech switch on H	S1 mech switch on H
	DC RPC type H (2)	DC RPC type H (2)
bit3	overtemperature H	overtemperature H
bit4	off control input H (3)	off control input H (3)
bit5	on control input H (3)	on control input H (3)
bit7	always 1	always 1
bit8	current (1)	tripped surge current H
bit9	current (1)	tripped fast trip H (4)
bit10	current (1)	spare
bit11	current (1)	spare
bit12	current (1)	tripped overcurrent (i^2t) H
bit13	current (1)	tripped undervoltage H
bit14	current MSB (1)	tripped grnd fault H
bit15	always 1	always 1

(1) RMS current

(2) If switch contains a mech. relay, then mech switch (on H / off L)
If DC RPC (no mech. relay), then DC RPC type (1 kW H / 3 kW L)

(3)

bit5	bit4	RPC command
0	0	on (error in hardware)
0	1	on
1	0	off
1	1	no change

(4) For DC RPC fast trip not flagged. DC RPC will be in "off" condition, but "commanded on" in fast trip situation.

GC Data Valid word format:

bit0 -> GC Data Valid switch 0 H
bit1 -> GC Data Valid switch 1 H
bit2 -> GC Data Valid switch 2 H
bit3 -> GC Data Valid switch 3 H
bit4 -> GC Data Valid switch 4 H
bit5 -> GC Data Valid switch 5 H
bit6 -> GC Data Valid switch 6 H
bit7 -> always 1
bit8 -> GC Data Valid switch 7 H
bit9 -> GC Data Valid switch 8 H
bit10 -> GC Data Valid switch 9 H
bit11 -> GC Data Valid switch 10 H
bit12 -> GC Data Valid switch 11 H
bit13 -> GC Data Valid switch 12 H
bit14 -> GC Data Valid switch 13 H
bit15 -> always 1

NOTE: L - data valid
H - data not valid

Sensorword Format:

bit0 -> sensor data bit 4
bit1 -> sensor data bit 5
bit2 -> sensor data bit 6
bit3 -> sensor data bit 7
bit4 -> don't care
bit5 -> don't care
bit6 -> don't care
bit7 -> always 1
bit8 -> sensor data bit 0
bit9 -> sensor data bit 1
bit10 -> sensor data bit 2
bit11 -> sensor data bit 3
bit12 -> don't care
bit13 -> don't care
bit14 -> don't care
bit15 -> always 1

A current/voltage sensorword_set consists of 9 sensorwords of the above format for a given current/voltage sensor. The 9 sensorwords will be of the following order:

V rms
I rms
V offset
I offset
V instantaneous
I instantaneous
P instantaneous
P real
frequency

In this document the notation sensorword_set_n will mean the 9 sensorwords of the described sensorword format in the described order for a given voltage/current sensor "n" where n can be sensor/voltage sensor 0 to 15

1) COMMAND: command switch off immediately even if already off or tripped

FORMAT: cc --> $20

dd1 --> $80 + j

j -- 7 bits corresponding to the switches as follows:

bit 0 -> switch 0
bit 1 -> switch 1
bit 2 -> switch2
bit 3 -> switch 3
bit 4 -> switch 4
bit 5 -> switch 5
bit 6 -> switch 6

dd2 --> $80 + k

k -- 7 bits corresponding to the switches as follows:

bit 0 -> switch 7
bit 1 -> switch 8
bit 2 -> switch 9
bit 3 -> switch 10
bit 4 -> switch 11
bit 5 -> switch 12
bit 6 -> switch 13

RESPONSE:- set up 2 sec timeout
- status as described in the NOTES

2) COMMAND: command switch on immediately even if already on or tripped

FORMAT: cc --> $21
dd1 --> $80 + j (j is defined in (1))
dd2 --> $80 + k (k is defined in (1))

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

3) COMMAND: reset switch
FORMAT: cc --> $22
dd1 --> $80 + j (j is defined in (1))
dd2 --> $80 + k (k is defined in (1))

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

4) COMMAND: select GC (all GC select codes will be set to zero)
FORMAT: cc --> $23
dd1 --> $86
dd2 --> $85

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

5) COMMAND: execute SIC firmware reset (does not reset actual set configuration)

FORMAT: cc --> $24
dd1 --> $80
dd2 --> $80

RESPONSE:
- set up 2 sec timeout
- four bytes of data plus the status as described in the NOTES where the first two bytes give the following data:

bit 0 -> 0 if GC0 connected, 1 if not
bit 1 -> 0 if GC1 connected, 1 if not
bit 2 -> 0 if GC2 connected, 1 if not
bit 3 -> 0 if GC3 connected, 1 if not
bit 4 -> 0 if GC4 connected, 1 if not
bit 5 -> 0 if GC5 connected, 1 if not
bit 6 -> 0 if GC6 connected, 1 if not
bit 7 -> always 1
bit 8 -> 0 if GC7 connected, 1 if not
bit 9 -> 0 if GC8 connected, 1 if not
bit 10 -> 0 if GC9 connected, 1 if not
bit 11 -> 0 if GC10 connected, 1 if not
bit 12 -> 0 if GC11 connected, 1 if not
bit 13 -> 0 if GC12 connected, 1 if not
bit 14 -> 0 if GC13 connected, 1 if not
bit 15 -> always 1

the third byte gives the following data:

bit 0 -> current SIC switch0 setting
bit 1 -> current SIC switch1 setting
bit 2 -> current SIC switch2 setting
bit 3 -> current SIC switch3 setting
bit 4 -> 0 if A/D connected, 1 if not
bit 5 -> don't care
bit 6 -> don't care
bit 7 -> always 1

the fourth byte gives the following data:

bit 0 -> don't care
bit 1 -> don't care
bit 2 -> don't care
bit 3 -> don't care
bit 4 -> don't care
bit 5 -> don't care
bit 6 -> don't care
bit 7-> always 1

6) COMMAND: reset continuous buffer

FORMAT: cc --> $25
dd1 --> $80
dd2 --> $80

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

7) COMMAND: fill continuous buffer (First use reset continous buffer then use this command to download code that is to be continuously executed. Code will start executing as soon as the download is started. Up to 80 of these commands may be concatenated before the buffer space is overrun.)

FORMAT: cc --> $26

ee1 --> $80 + q (q is defined as higher 4 bits of 8-bit code(see sensorword))

ee2 --> $80 + r (r is defined as lower 4 bits of 8-bit code (see sensorword))

At the end of the command is appended a $26 until the last command, then a $0D is appended.

RESPONSE: - set up 2 sec timeout

- status as described in the NOTES

8) COMMAND: fill once buffer (This command is used to download code that is to be executed only once. Code execution is started by the trigger once buffer command. Up to 80 of these commands may be concatenated before the buffer space is overrun.)

FORMAT: cc --> $27
ee1 --> $80 + q (q is defined as (13))
ee2 --> $80 + r (r is defined in (13))
ee3 --> as defined in (13)

At the end of the of the command or commands is appended a $0D.

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

9) COMMAND: get buffered data

FORMAT: cc --> $29

dd1 --> $80 + v

(v is defined as:

bit0 -> buffer0

bit1 -> buffer1

bit2 -> buffer2

bit3 -> buffer3

bit4 -> don't care

bit5 -> don't care

bit6 -> don't care)

dd2 --> $80

RESPONSE: - set up 2 sec timeout

- data of the following format and status as described in NOTES

HEADER - $20

$ssssss - three bytes of status

$8F - dip switch setting for SIC card (if not $8F, SIC card not installed)

$nnnn - position in loop counter

$kk - times through loop counter

$mm - breakpoint

$22 - start of data

--> 14 switchwords plus 1 GC Data Valid word

NOTE:	TM is temperature multiplexed, TC is temperature common (TM is not useful)	temperature sensorwords 0TM, 0TC, 1TM, 1TC, 2TM, 2TC, 3TM, 3TC
		frequency sensorword 0
		sensor_word_set_0
		frequency sensorword 1
		sensor_word_set_1
		frequency sensorword 2
		sensor_word_set_2
		frequency sensorword 3
		sensor_word_set_3
	--->	$22 - end of buffer
		repeat arrowed sections for sensors 4 to 7, 8 to 11, and 12 to 15

10) COMMAND: trigger once buffer
FORMAT: cc --> $2A
dd1 --> $80
dd2 --> $80

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

11) COMMAND: get power factor and sign (To calculate the power factor use pf1=[Pavg1/[Vrms1*Irms1]. Use the same calculation to determine pf2 using Pavg2, Vrms2, and Irms2; if pf2 < pf1 denotes capacitive loading; if pf2>=pf1 denotes inductive loading; ie, voltage leading current)

FORMAT: cc --> $2B
dd1 --> $80 + j (j is defined as 0 to $F depending on sensor pair used)
dd2 --> $80

RESPONSE: - set up 2 sec timeout
- data defined as six sensor words for the specified in the following order plus status as described in the NOTES.

V rms1
I rms1
P real1
V rms2
I rms2
P real2

12) COMMAND: get data for one specified switch a specified number of times

FORMAT: cc --> $2C

dd1 --> $80 + j (j is defined as 1 to $7F depending on the number of times data is specified to be taken -- input buffer must be taken into account)

dd2 --> $80 + k (k is defined as 0 to $D depending on the switch specified)

RESPONSE: -set up 2 sec timeout

- data defined as:

j number of 16-bit switchwords plus the status as described in the notes

13) COMMAND: get data for one specified sensor a specified number of times

FORMAT: cc --> $2D

dd1 --> $80 + j (j is defined as 1 to $EF depending on the number of times data is specified to be taked)

dd2 --> $80 + k (k is defined as 0 to $F depending on the sensor specified)

RESPONSE: - set up 2 sec timeout

- data defined as:

j number of sensorword_set_n for the specified sensor plus the status as described in the NOTES

14) COMMAND: command switch on checking switch on or tripped status first; if any of the above conditions exist, the switch command for that particular switch or switches is not executed

FORMAT: cc --> $2E
dd1 --> $80 + j (j is defined in (1))
dd2 --> $80 + k (k is defined in (1))

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

15) COMMAND: command switch off checking switch off or tripped status first; if any of the above conditions exist, the switch command for that particular switch or switches is not executed

FORMAT: cc --> $2F
dd1 --> $80 + j (j is defined in (1))
dd2 --> $80 + k (k is defined in (1))

RESPONSE: - set up 2 sec timeout
- status as described in the NOTES

16) COMMAND: get data for all fourteen switches a specified number of times.

FORMAT. cc --> $30

dd1 --> $80 + j (j is defined as 1 to $7F depending on the number of times data is specified to be taken, input buffer size must be taken into account)

dd2 --> $80

RESPONSE: - set up 2 sec timeout

- data defined as:

(j times (fourteen switchwords plus GC Data Validword set)) plus the status as described in the NOTES

17) COMMAND: get data for all sixteen sensors one time
FORMAT: cc --> $31
dd1 --> $80
dd2 --> $80

RESPONSE: - set up 2 sec timeout
- data defined as:
sixteen sensorword_set_n plus status
as described in the NOTES

18) COMMAND: get all 16 temperature sensor readings one time
FORMAT: cc --> $32
dd1 --> $80
dd2 --> $80

RESPONSE: - set up 2 sec timeout
- 16 * 2 sensorwords for the temperature sensors and the status as described in the NOTES

19) COMMAND: get all 16 power factors and signs
(To calculate the power factors see (17))

FORMAT: cc --> $33
dd1 --> $80
dd2 --> $80

RESPONSE: - set up 2 sec timeout
- data defined as 16 * (six sensor words for each sensor in the following order) plus the status as described in the NOTES.

V rms1
I rms1
P real1
V rms2
I rms2
P real2

APPENDIX III

20 kHz AC Remote Power Controller Equipment Specification Document

This equipment specification document describing the operation of a 20 kHz AC Remote Power Controller was prepared for reference use only by Martin Marietta and does not specifically refer to the breadboard units developed for the SSM/PMAD.

REVISIONS

REV	SH	DESCRIPTION	DATE	APPR

DRAWING NO.

REV	
SH	

REV STA
OF SHEE

DRAWN BY	DEPT	DATE
S. McKay		9-13-86
CHECKER		
GR ENGR		
PROJECT		
CONTRACT NO		

MARTIN MARIETTA CORPORATION
DENVER AEROSPACE. POST OFFICE BOX 179. DENVER. COLORADO 80201

20 KHZ AC REMOTE POWER CONTROLLER

SIZE	FSCM NO.	DWG NO	
A	04236	NSR/A875CR215950	
SCALE III-2			SHEET

ERUNING 44-141 37784-21

REVISIONS

SYM	PAGE	DESCRIPTION	DATE	APPROVED

CHG	SIZE	CODE IDENT NO.	MARTIN MARIETTA CORP.
			NSR/A875CR215950
	SCALE	PAGE	SHEET 1

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1.0 SCOPE

1.1 General This Drawing establishes the design, construction, performance, and verification requirements for Remote Power Controller. Hereinafter the Remote Power Controller is referred to as the RPC.

1.2 Classification The RPC shall be designated by Controlling Specification Number(s) as follows:

DASH NUMBER	NOMENCLATURE
875CR215950	20 Khz AC Remote Power Controller

2.0 APPLICABLE DOCUMENTS

2.1 General The following documents of the exact issue shown shall form part of this drawing to the extent specified herein. When an exact issue is not specified, the applicable issue shall be as required in the Procurement Agreement. In case of conflict between the requirements of this drawing and any referenced document, the requirements of this drawing shall govern.

2.1.1 Specifications

2.1.1.1 Federal

2.1.1.2 Military

MIL-B-5087B 15 Oct 64 Int Amend 3 24 Dec 84 Amend 2 31 Aug 70	Bonding, Electrical and Lightning Protection for Aerospace Systems
MIL-P-9024G 06 Jun 72	Packaging, Handling and Transportability In System/Equipment Acquisition
MIL-A-21180D 05 Nov 84	Aluminum Alloy Castings, High Strength

3.1.1.3 Other

SP-R-0022A 9 Sept 74	Vacuum Stability Requirements of Polymeric Materials for Spacecraft Applications.
MSFC-STD-512A 01 Dec 76	Man/System Requirements for Weightless Environments
NASA RP-1024 July 1978	Anthropometric Sourcebook
JSC 30000	Space Station Program Definition and Requirements
MSC S-M-0003	Design Requirements/Manned Spacecraft and Related Flight Crew Equipment Markings, Labling and Color
SS-SRD-0001	

2.1.2 Standards

2.1.2.1 Federal

FED-STD-101C 13 Mar 80 Change Notice 1 08 Oct 82 Change Notice 12 Sep 83	Test Procedures for Packing Materials
FED-STD-209B(1) 24 Apr 73 Amend 1 30 May 76	Clean Room and Work Station Requirements, Controlled Environment
FED-STD-595A Notice 9 29 May 85 Notice 8 30 Aug 84 Notice 7 01 Jan 84 Notice 6 01 Feb 80 Notice 5 01 Mar 79 Notice 4 01 Aug 73 Notice 3 28 Apr 72 Notice 2 17 Apr 72 Notice 1 02 Jan 68	Colors

2.1.2.2 Military

MIL-STD-129J 25 Sep 84	Marking For Shipment and Storage
MIL-STD-130F 21 May 82 Notice 1 2 July 84	Identification Marking of US Military Property
MIL-STD-461B 01 Aug 80	Electromagnetic Emission and Susceptibility Requirements for the Control of Electromagnetic Interference
MIL-STD-470A 03 Jan 83	Maintainability Program for Systems and Equipment
MIL-STD-1472C 02 May 81	Human Engineering Design Criteria for Military Systems, Equipment and Facilities

MIL-STD-1522A 28 May 84 Notice 1 21 Dec 84	Standard General Requirements For Safe Design and Operation of Pressurized Missile and Space Systems
MS33540G 09 Feb 73	Safety Wiring, and Cotter Pinning, General Practices for

2.1.2.3 Industry

ANSI Y14.5M 1982	Dimensioning and Tolerancing
ANSI Y32.2 1975	Graphic Symbols for Electrical and Electronics Diagrams
ANSI Y32.16 1975	Reference Designations for Electrical and Electronics Parts and Equipment

2.1.2.4 Occupational

2.1.3 Other Publications

2.1.3.1 Manuals

2.1.3.2 Regulations

2.1.3.3 Handbooks

MIL-HDBK-5D 1 Jun 83 Vol 1 Notice 1 1 Jan 84 Vol 2 Notice 2 1 Jan 84	Metallic Materials and Elements for Aerospace Vehicle Structures
NHB 6000.1C	Requirements for Packaging, Handling and Transportation for Aeronautical and Space Systems Equipment and Associated Components

2.1.3.4 Martin Marietta Denver Aerospace

M-67-45 Revision 3 Dec 83	Test Methods and Controls Components
SSP-MMC-00020 WP-01 Vol 1	Systems Test and Verification Plan

3.0 REQUIREMENTS

3.1 Item Definition. A RPC is a solid state remote power controller and a circuit monitoring and protection device. This specification defines the requirements of solid state RPC for use in protecting the 208 Vac, 20 KHz electrical distribution system from overloads and faults. The RPC covered by this specification will be used for protection of BUS feeders as well as the wiring to individual loads. Coordination between RPC's of differing rating is required. RPC operation shall be trip free. RPC shall be capable of Ground Fault interruption.

3.2 Characteristics The RPC shall be SPST and shall be designed to actuate by means of logic level signal applied to the on and off control inputs. The RPC control inputs will also have a inhibit and data enable described herein. These inputs will be from open collector sources with a maximum 36V off state voltage, sinking capability of 10 mA in the low state and a maximum leakage current of 100 uA in the high state. A tripped device shall be reset by removing and reapplying the control signal. T[redacted] voltage [redacted] (Figure 2). The RPC shall be capable of actuating a latching type load isolation relay which will electrically isolate the load by switching the relay off after the RPC has turned off. Similarly, the RPC shall turn the relay on prior to initiating its normal turn on function. Two RPCs shall be compatible in forming a break-before-make SPDT switch. The control circuit shall be electrically isolated from the power circuits, the control circuitry will receive power from the primary line. [redacted]

3.2.1 Performance Characteristics. The performance characteristics of the RPC shall be as specified in the following paragraphs.

3.2.1.1 Power

3.2.1.1.1 Power input. The RPC shall meet the requirements of this drawing when operating on input power with the following characteristics:

Frequency	20 KHz +/- .5% Hz	
Voltage	208 Vrms	+/- 2.5% at Modules and attached payloads
Load Power Factor	0.9 Min	
Total Harmonic Distortion	3%	Maximum amplitude: 3rd harmonic 30 db below fundamental. 5th harmonic (TBS) db below fundamental

3.2.1.1.1.1 Power Consumption

Switch Currents (switch off with rated load connected)	3ma at 208 Vac 20 Khz
Supply Current (100% rated load)	Load current +3mA at 208 Vac 20 KHz

3.2.1.3.1 Power Switch The solid state power switch shall operate within the following characteristics.

A)	Switch Form	SPST
B)	Trip Characteristics	Figure 1.
C)	Switch Ratings	Table 6
D)	Overload Trip	1.1 x Rating (Figure 1)
E)	Fault Trip	4.3 x rating (max) within 5ms.
F)	Peak Let-thru current	4.3 x rating (max)
G)	Rupture Current	Unlimited (current limited)
H)	On-state voltage drop	1.15 Vac (max)
I)	Power Dissipation*	1% of VA rating (max)
J)	Turn-on/turn-off delay	2.5 ms (Max)
K)	Turn-on	within 2uS of zero
L)	Turn-off	within 2uS of zero current
M)	Initial Turn-on or restart current limit	2.25± .25 x rating
N)	Initial Turn-on or restart time delay	50± 5 msec to 5± .5 sec selectable

* A design goal is to minimize the power dissipation in the RPC power stage.

3.2.1.3. Trip Characteristics (Figure 1)

3.2.1.3.1 Overload The RPC shall automatically attempt a second start-up any time the load current exceeds the time/current envelope of Figure 1.

3.2.1.3.2 Initial Turn-On The RPC shall limit the inrush curent to 225%± 25% of its rating for a fixed time delay during initial turn-on or re-start. The fixed time delay shall be adjustable from a minimum of 50 milliseconds to 5 seconds maximum. An external capacitor may be used to set the time delay. An external resistive element may also be used in order to minimize the heat dissipation internal to the RPC in the current limit mode.

3.2.1.3.3 Load Faults The RPC shall provide load fault verification and fuse backup in the event that the trip circuit fails to operate.

3.2.1.3.4 Reset A tripped RPC shall be reset by cycling the control signals OFF then ON.

3.2.1.3.5 Ground Fault A common mode current on the input power lines exceeding 50 mA for 40 mS shall cause the RPC to trip off.

3.2.1.3.6 Power Supply Surges A power supply surge that results in a current surge that exceeds the trip curve of Figure 1 shall result in the RPC automatically restarting its turn-on sequence.

3.2.1.3.7 Power Supply Blackout A power supply that drops below 150 volts for more than 2.5 milliseconds shall cause the RPC to switch off at the subsequent zero current crossing. When the power supply returns to normal, the RPC shall automatically restart its turn-on sequence.

3.2.1.4 Control Circuits

3.2.1.4.1 Logic Levels Logic levels shall be as noted in the following table:

Logic State	Logic Level	Logic Voltage
Low	0	-0.5 to +2.5 Vdc
High	1	+3.5 to +36 Vdc

Output circuits shall be of the "open collector" type capable of sinking -10 mA in the LOW state and having a maximum leakage current of -100 uA in the HIGH state (with 36 Vdc applied through a 3600 ohm resistor). Input circuits shall be capable of interfacing with TTL, CMOS or open collector circuits. For open collector inputs, the internal pull-up circuit shall be capable of supplying at least 100 uA in the HIGH state. The LOW state sink current shall not exceed 10 mA.

3.2.1.4.2 ON/OFF Control Inputs The RPC shall have separate ON and OFF inputs that control the RPC's power switch as described in the following table:

ON Input	OFF Input	RPC Status
0	0	ON
0	1	ON
1	0	OFF
1	1	NO CHANGE

Each input shall be capable of accepting either a continuous or a pulsed logic LOW input. For a pulsed input, the minimum pulse width shall be 10 milliseconds with a rise and fall time of less that 1 millisecond.

3.2.1.4.3 INHIBIT Input The INHIBIT input shall turn off the RPC's power switch but shall not change the state of the internal latch set by the ON/OFF inputs.

Inhibit Input	RPC Response
LOW State	Power Switch Inhibited
HIGH State	Power Switch Enabled

3.2.1.4.4 DATA ENABLE The RPC shall generate a serial data output as described in paragraph 3.2.15.2 in response to the DATA ENABLE and CLOCK inputs. Refer to Figure 5.

Data Enable Input	RPC Response
LOW State	Data Latched (1)
HIGH State	Data Unlatched, RPC reset (2)

(1) Transmission begins on first falling edge of CLOCK pulse (paragraph 3.2.1.4.5).

(2) Ceases data transmission. Data transmission commences with MSB upon next RPC interrogation.

3.2.1.4.5 CLOCK The RPC shall accept a 115.2 kHz clock (Figure 5) for bit timing of the SERIAL DATA OUTPUT (paragraph 3.2.1.5.2). The RPC shall transmit a serial data output as described in paragrah 3.2.15.2 in response to the falling edge of each CLOCK pulse when the DATA ENABLE (paragraph 3.2.1.4.4) is in a LOW state.

3.2.1.4.7 Load Isolation Relay/Contactor Coil Drive and Position Monitor Circuits - TBD

3.2.1.5 Monitor Circuits

3.2.1.5.1 Logic Levels - Same as paragraph 3.3.5.1.

3.2.1.5.2 Serial Data Output - The RPC shall transmit serial data in accordance with Table 5 in response to the DATA ENABLE (paragraph 3.2.1.4.4) and CLOCK (paragraph 3.2.1.4.5) inputs. The SERIAL DATA OUTPUTS of TBD RPC's shall be capable of being paralleled, forming a single serial data output bus. The SERIAL DATA OUTPUT shall be synchronized to an external clock signal (paragraph 3.2.1.4.5) and will shift data to the left (Figure 5) beginning with bit 15 (MSB) on the falling edges of the CLOCK pulses. The RPC shall be interrogated in accordance with the timing diagram depicted in Figure 5.

3.2.1.5.2 STATUS DISCRETE - The STATUS DISCRETE output shall indicate the state of the RPC power switch.

RPC Power Switch State	STATUS DISCRETE Output State
ON	LOW
OFF	HIGH

3.2.1.6 RPC Loads - The RPC shall be capable of powering the following load mix:

1. Resistive loads
2. Inductive loads
3. 20 kHz transformers
4. Off-line bridge rectifiers (Figure 4)

3.2.2 Physical Characteristics

3.2.2.1 Size and Configuration The size, configuration and mounting dimensions shall be in accordance with the requirements of figure TBD (see 3.3.11 herein - dimensioning and tolerancing).

3.2.2.2 Weight The RPC shall be designed to a minimum weight but shall not exceed .6 lb. for a 15 amp RPC.

3.2.2.3 Mounting The RPC shall operate as specified herein when mounted in any orientation.

3.2.2.4 Electrical Interface. The electrical interface diagram for the RPC is shown in Figure 2.

3.2.3 Reliability

3.2.3.1 Design Requirements Reliability requirements and criteria shall be established and incorporated into the design. The effective implementation of these requirements shall be accomplished as specified herein.

3.2.3.2 Supplier Reliability Program. The supplier shall establish a reliability program that meets the requirements of JSC 30000, Section 9, paragraph 3.0. The reliability program shall be an integral part of the supplier's design, development, test and operational activities.

3.2.3.3 Field Reliability The RPC shall achieve a meantime between failures (MTBF) of at least TBS hours. The MTBF shall be based on an operating time of TBS hours per year and a non-operating (standby) time of TBS hours per year. If redundancy is required to achieve the specified reliability it shall be subject to Martin Marietta approval.

3.2.3.4 Failure Tolerance N/A

3.2.3.5 Failure Propagation The RPC design shall be such that one failure does not cause additional failures.

3.2.3.6 Service Life The RPC shall remain operational 10 years before replacement is needed.

3.2.4 Maintainability Design for maintainability shall be in accordance with JSC 30000, Section 3, Part (TBD), (SSP-MMC-#TBD Maintainability Implementation Plan) and (SSP-MMC-#TBD Maintainability Design Guide). Design for maintainability includes but is not limited to requirements for access, meantime to repair (MTTR), fasteners, mounting interface and maintainability verification.

3.2.4.1 Maintenance Concept The maintenance concept is specified in JSC 30000, Section 4, Part 4.

3.2.5 Environmental Requirements

3.2.5.1 Ground storage, transportation and handling environments The assembly shall meet the requirements specified herein after exposure in a packaged (unless otherwise specified), non-operating condition to the following environments.

3.2.5.1.1 Temperature -55° to 65°C (-67°F to 149°F).

3.2.5.1.2 Pressure 20.6 kPa to 110 kPa (3 psia to 16 psia)./

3.2.5.1.3 Relative Humidity 0 - 100%.

3.2.5.1.4 Salt fog 1% NaCl by weight, as defined in MIL-STD-810, method 509.2, Procedure 1.

3.2.5.1.5 Fungus As identified in MIL-STD-810, method 508.3.

3.2.5.1.6 Ozone 10 parts per billion by volume.

3.2.5.1.7 Thermal Radiation As defined in MIL-STD-810, Method 505.2, procedure I.

3.2.5.1.8 Sand and Dust TBD

3.2.5.1.9 Sinusoidal Vibration As defined in Marshall TM86538 Section VI, Transportation and Handling Criteria and Procedures.

3.2.5.1.10 Acceleration (covered under 3.2.5.1.9 and 3.2.5.1.10.1).

3.2.5.1.10.1 Vibration Criteria The transportation vibration criteria are presented in paragraphs (a) through (d) for the various modes of transporcation. When testing is performed, the vibration test frequencies are swept logarithmically from 5 Hz. to the maximum frequency and back to 5 Hz at 1 octave per minute in each axis. The components should be instrumented to determine major resonances. A 15 minute sinusoidal dwell is required at each major component resonance at the criteria amplitude specified for the sweep test. Criteria below 5 Hz are for design considerations only and no test is required. The criteria are tabulated below:

(a) Aircraft

(1) Jet (5-2000-5 Hz @ 1 oct/min)
5 - 10 Hz @ 0.022 in. D.A. Disp.
10 - 35 Hz @ 0.11 g's peak
35 -200 Hz @ 0.0017 in. D.A. Disp.
200-2000 Hz @ 3.5 G's peak

(2) Propeller (5-700-5 Hz @ 1 oct/min)
2 - 4 Hz @ 0.42 in. D.A. Disp.*
4 - 5 Hz @ 0.35 g's peak*
5 -12 Hz @ 0.35 g's peak.
12 -55 Hz @ 0.045 in. D.A. Disp.
55-300 Hz @ 7.0 g's peak
300-700 Hz @ 3.5 g's peak

(3) Helicopter (5-600-5 Hz @ 1 oct/min)
5 - 12 Hz @ 0.22 in. D.A. Disp.
12 - 40 Hz @ 1.6 g's peak
40 - 55 Hz @ 0.019 g's peak
55 -120 Hz @ 3.0 g's peak
120 -170 Hz @ 0.0040 in. D.A. Disp.
170 -220 Hz @ 6.0 g's peak
220 -260 Hz @ 0.0024 in. D.A. Disp.
260 -600 Hz @ 8.0 g's peak

(b) Truck

(1) Smooth Paved Roads (5-300-5 Hz @ 1 oct/min)
1 - 4 Hz @ 0.43 in. D.A. Disp.*
4 - 5 Hz @ 0.35 g's peak*
5 -150 Hz @ 0.35 g's peak
150 -300 Hz @ 0.06 g's peak

(2) All Road Conditions (5-1000-5 Hz @ 1 oct/min)
1 - 7 Hz @ 1.7 g's peak*
7 -15 Hz @ 1.7 g's peak
15-1000 Hz @ 1.7 g's peak

(c) Trains

(1) Normal Railroad operations (5-2000-5 Hz @ 1 oct/min)

2 - 3 Hz @ 2.6 in.D.A. Disp.*
3 - 6 Hz @ 1.2 g's peak*
6 - 130 Hz @ 1.2 g's peak
130 - 185 Hz @ 0.0014 in. D.A. Disp.
185 - 2000 Hz @ 2.5 g's peak

(d) Ships

(1) Normal Shipping Operations (5-300-5 Hz @ 1 oct/min)

0.1 - 0.3 Hz @ 0.35 g's peak*
0.3 - 1.5 Hz @ 0.35 g's peak*
1.5 - 4.0 Hz @ 0.10 g's peak*
4.0 - 5.0 Hz @ 0.12 in. D.A. Disp.
5.0 - 11 Hz @ 0.12 in. D.A. Disp.
11 - 300 Hz @ 0.75 g's peak

* Design criteria only, no test required.

3.2.5.1.11 Shock As defined in Marshall TM86538 Section VI Transportation and Handling Criteria and Procedure.

3.2.5.1.11.1 Shock Criteria, Transportation When shock testing is required because of rail shipment the test should be conducted by applying five shocks in each of three mutually perpendicular axes (15 shocks total). Any shock pulse that results in a response spectrum (Q= 10) as severe as that presented below will be acceptable.

Railroad Car Humping Conditions (5 shocks per axis)

20 - 160 Hz @ +6 dB/oct
160 - 340 Hz @ 500 G's peak
340 - 400 Hz @ -6 dB/oct

3.2.5.1.11.1 Transportation Shock Handling Criteria and Procedures Handling criteria are required to account for typical conditions that occur during loading or unloading operations. Tests for these conditions consist of numerous container drops from various orientations of the container. Where equipment design allows, equipment will be subjected to a transit drop test as described below. If normal equipment design does not allow this type testing, the procedures and required protection in handling are to be submitted to the appropriate MSFC program manager for approval.

3.2.5.1.11.2 Test Conditions The transit drop test should be used for equipment in its transit or combination case as prepared for field use to determine if the equiment is capable of withstanding the shocks normally induced by loading and unloading of equipment.

For equipment weighing 1000 pounds or less, the floor or barrier receiving the impact shall be of solid 2-in. thick plywood backed by either concrete or a rigid steel frame. For equipment weighing over 1000 pounds, the floor or barrier shall be concrete or its equivalent.

3.2.5.1.11.4 Test Performance. Subject the test item to the number and heights of drop as indicated in Table 3.2.5.1.11.4-1. Prior to proceeding with any of the test methods, the test item shall be operated under standard ambient conditions and a record made of all data necessary to determine compliance with required performance. These data shall provide the criteria for checking satisfactory performance of the test item, either during or at the conclusion of the test, or both, as required.

Thale 3.2.5.1.11.4-1

Weight and Test Item and Case (pounds)	Largest Dimensions (inches)	Notes	Height of Drop (inches)	Number of drops
Under 100 lb. Man-Packed and Man-Portable	Under 36	A	48	Drop on each face, edge, and corner.
	36 & over	A	30	Total of 26 drops.
100 to 200 lb Inclusive	Under 36	A	30	Drop on each corner.
	36 & over	A	24	
Over 200 to 1000 lb Inclusive	Under 36	A	24	
	36 to 60	B	36	Total of 8 drops.
	Over 60	B	24	
Over 1000	No limit	C	18	4 edgewise drop. 2 cornerwise drops.

Note A. Drops shall be made from a quick-release hook or drop tester as made by the L.A.B. Corporation, Skaneateles, New York, or equal. The test item shall be oriented so that upon impact a line from the struck corner or edge to the center of gravity of the case and contents is perpendicular to the impact surface.

Note B. With the longest dimension parallel to the floor, the transit or combination case with the test item within shall be supported at the corner of one end by a block 5 in. high and at the other corner or edge of the same end by a block 12 in. high. The opposite end of the case shall then be raised to the specified height at the lowest unsupported corner and allowed to fall freely.

Note C. While in the normal transit position, the case and contents shall be subjected to the edgewise and cornerwise drop test as follows (if normal transit position is unknown, the case shall be oriented such that the two longest dimensions are parallel to the "floor").

Edgewise drop test. One edge of the base shall be supported on a sill 5 to 6 in. high. The oposite edge shall be raised to the specified height and allowed to fall freely. The test shall be applied once to each edge of the base of the case (total of four drops).

Cornerwise drop test: One corner of the base of the case shall be supported on a block approximately 5 in. high. A block normally 12 in. high shall be placed under the other corner of the same end. The opposite end of the case shall be raised to the specified height at the lowest unsupported corner and allowed to fall freely. This test shall be applied once to each of two diagonally opposite corners of the base (total of two cornerwise drops). When the proportions of width and height of the case are such as to cause instability in the cornerwise drop test, edgewise drops shall be substituted. In such instances two more edgewise drops on each end shall be performed (four additional edgewise drops for a total of eight edgewise drops).

(b) Upon completion of the transit drop test, the test item shall be operated and the results compared to data obtained prior to testing in accordance with the following procedures. Prior to proceeding with any of the test mehtods, the test item shall e operated under standard ambient conditions and a record made of all data necessary to determine compliance with required performance. These data shall provide the criteria for checking satisfactory performance of the test item during testing or at the conclusion of the test or both, as required. CErtification by signature and data block is required.

(c) The test item shall then be visually inspected and a record made of any damage/deterioration resulting from the test. If a test chamber is used for the test, perform a visual inspection of the test item within the chamber at test conditions when possible. Upon completion of the test, visually inspect the test item again after the test item has been returned to standard ambient conditions. Deterioration, corrosion, or change in tolerance limits or any internal or external parts which could in any manner prevent the test item from meeting operational service or maintennance requirements shall be reason to consider the test iter as having failed to withstand the conditions of the test.

3.2.5.2 Launch environments The assembly shall meet the requirements of this specification during and after exposure to the following launch environments.

3.2.5.2.1 Module Interior

3.2.5.2.1.1. Temperature +15.6° to 32.2°C (60°F to 90°F)

3.2.5.2.1.2 Pressure 100 to 013 kPa (14.5 tol4.9 psia)

3.2.5.2.1.3 Humidity 1.7°C to 21°C dew points (35°F to 70°F)

3.2.5.2.1.4 Airborn NaCl TBD

3.2.5.2.1.5 Fungus 1000 coony forming units (CFU)/m^3.

3.2.5.2.1.6 Ozone 6 parts per billion by volume.

3.2.5.2.1.7 Sand and Dust TBD

3.2.5.2.1.8 Random Vibration See Figure 3.2.5.2.1.8-1 through 3.2.5.2.1.8-2 for input random vibration levels at attach point and for the response load factors as a function of fundamental frequency for design.

3.2.5.2.1.9 Acceleration Covered in 3.2.5.2.1.8 and 3.2.5.2.1.11.

3.2.5.2.1.10 Acoustics See Table 3.2.5.2.1.10-1.

Table 3.2.5.2.1.10-1

1/3 Octave Center Frequency (Hz)	Band Level (dB re 2 x 10 $^{-5}$N/n^2)
31.5	111.0
40	113.0
50	116.0
63	118.5
80	120.0
100	122.0
125	124.0
160	125.0
200	126.5
250	127.0
320	127.0
400	127.0
500	126.0
630	123.5
800	120.5
1000	115.5
1250	113.5
1600	112.0
2000	109.0
2500	106.5
3200	103.0
4000	100.5
5000	97.5
6300	95.0
8000	91.0
10000	89.0
OAL	136.0

TEST TIME: TBD

3.2.5.2.1.11 Transient Vibration See Table 3.2.5.2.1.11-1. Lift off transient load factors shall be combined with vibroacoustic load factors as shown in 3.2.5.2.1; however landing transient load factors are totals.

Table 3.2.5.2.1.11-1
Transient Vibration

	LIFTOFF			LANDING		
ITEM/COMPONENT	X g's	Y g's	Z g's	X g's	Y g's	Z g's
RACK/STRUCTURE	3.0/-6.0	+5.0	+5.0	+5.0	+5.0	6/-4.0
COMPONENTS	4.0/-7.0	+6.0	+6.0	+6.0	+6.0	7/-5.0

NOTES

1. Load factors are provided in Orbiter coordinate axes.

2. Items/comonents mounted directly to the module primary structure (including the integrated racks) should have a minimum natural frequency greater than 25 Hz.

3. Items/components mounted to secondary support structure, such as a rack, should have a minimum natural frequency greate than 35 Hz.

3.2.5.2.1.12 Loads Combination The transient/steady state load/factors are assumed to act simultaneously resulting in correlated loads. Loads due to random vibration shall be assumed to be uncorrelated, acting in any direction, but only one direction at a time. Limit loading for secondary structure and comonents is based on superposition of transient/steady state (T/SS) and random vibration (R) or acoustic (A) loads:

$$L_{limit} = L_{T/SS} + L_R$$

or, for large surface area, lightweight structure,

$$L_{limit} = L_{T/SS} + L_A.$$

Random Vibration Criteria

20 Hz	.006 g^2/Hz
20 - 100 Hz	3 dB/octave
100 - 200 Hz	.03 g^2/Hz
200 - 300 Hz	-3 dB/octave
300 -1000 Hz	.02 g^2/Hz
1000 -2000 Hz	-9 dB/octave
2000 Hz	.0025 g^2/Hz

Composite = 5.3 g rms

Random Vibration Load Factors

Figure 3.2.5.2.1.8-1 Zone CM-1 Common Module Cylinder Wall Ring Frame/Longeron Junctions

Random Vibration Criteria

	20 Hz	.002 g^2/Hz
20 -	100 Hz	+5 dB/octave
100 -	600 Hz	.03 g^2/Hz
600 -	2000 Hz	-6 dB/octave
	2000 Hz	.0028 g^2/Hz

Composite = 5.34 g rms

Random Vibration Load Factors

Figure 3.2.5.2.1.8-2: Zone CM-2 Common Module Cone Sections

Table 3.2.5.2.2.6-1
Orbiter Cargo Bay Combined Liftoff/Boost Acoustic Spectrum

1/3 Octave Band Center Frequency (Hz)	Sound Pressure Level (dB) Ref. 2 x 10-5N/M2
20.0	118.0
25.0	120.0
31.5	122.0
40.0	124.0
50.0	125.5
63.0	127.0
80.0	128.0
100.0	128.5
125.0	129.0
160.0	129.5
200.0	129.0
250.0	129.0
315.0	128.5
400.0	127.5
500.0	125.0
630.0	123.0
800.0	121.0
1000.0	119.0
1250.0	117.5
1600.0	116.0
2000.0	114.0
2500.0	112.0
3150.0	110.5
4000.0	108.5
5000.0	106.5
6300.0	105.0
8000.0	103.0
10000.0	101.0
OVERALL SPL	139.0

3.2.5.3 Orbital Operational Environments The assembly shall meet the requirements specified herein during and after exposure to the following environments.

3.2.5.3.1 Orbital Internal Environments

3.2.5.3.1.1 Temperature 18°C to 24°C (65°F to 75°F) nominal: 15.6°C to 29°C (60°F to 85°F) 28 day degraded; 19.6°C to 32.2°C (60°f to 90°F) emergency; TBD during emergency decontamination.

3.2.5.3.1.2 Pressure 100 to 103 kPa (14.5 to 14.9 psia) nominal; 1.3 x 10^{-8} kPa (10^{-10} torr) during emergency decontamination.

3.2.5.3.1.3 Humidity 4°C to 10°C dewpoints (40°F to 50°F) nominal; 1.7°C to 32°C dewpoints (35°F to 70°F) 28 day degraded.

3.2.5.3.1.4 Random Vibration 15-1000 @ .003 g/Hz
1000-2000 @ 6 dB/oct.

3.2.5.3.1.5 Acoustics All areas for hearing conservation purposes shall not exceed: LEQ 100 dB. Noise peaks, regadless of duration, cannot exceed 30 dB over the baseline noise specification.

3.2.5.3.1.6 Acceleration

3.2.5.3.1.7 Radiation TBD.

3.2.5.3.1.8 Transient Vibration 0-20 Hz @ 0.26 g/0 peak.

3.2.5.3.1.9 Loads Combination See 3.2.5.3.1.12.

3.2.5.3.2 Orbital External Environments

3.2.5.3.2.1 Thermal Radiation

3.2.5.3.2.1.1 Solar Radiation 1371 +/-5W/m^2.

3.2.5.3.2.1.2 Earth Albedo 30%.

3.2.5.3...1.3 Earth Emitted Radiation 237 W/m^2.

3.2.5.3.2.1.4 Space Sink Temperature 3K (-270°C).

3.2.5.3.2.2 External Pressure 2 X 10^{-7} to 1.3 x 10^{-8} kPa (1.5 x 10^{-9} torr to 1 x 10^{-10} torr).

3.2.5.3.2.3 Random Vibration TBD.

3.2.5.3.2.4 Acceleration TBD.

3.2.5.3.2.5 Particle Radiation

3.2.5.3.2.5.1 Ionosphere Plasma TBD.

3.2.5.3.2.5.2 Trapped Radiation TBD.

3.2.5.3.2.5.3 Solar Cosmic Rays TBD.

3.2.5.3.2.5.4 Galactic Cosmic Rays TBD.

3.2.5.4 Orbital Operation Environments The MSU shall meet the requirements specified herein during and after exposure to the following environments.

3.2.5.4.1 Orbital Internal Environments

3.2.5.4.1.1 Temperature 18°C to 24° (65°F to 75°F) nominal; 15.6°C to 29°C (60°F to 85°F) 28 day degraded; 19.6°C to 32.,2°C (60°F to 90°F) emergency; TBD during emergency decontaminaion.

3.2.5.4.1.2 Pressure 100 to 013 kPa (14.5 to 14.9 psia) nominal; 1.3×10^{-8} kPa (10^{-10} torr) during emergency decontamination.

3.2.5.4.1.3 Humidity 4°C to 10°C dewpoints (40°F to 50°F) nominal; 1.7°C to 21°C dewpoints (35°F to 70°F) 28 day degraded.

3.2.5.4.1.4 Random Vibration 15-1000 @ .003 g^2/Hz.
1000-2000 @ -6 dB 1 oct.

The structure shall be capable of operating without structure damage under these levels for 30 years.

3.2.5.4.1.5 Acoustics Component acoustic output cannot exceed

Leq (24) _ 70 dBA hearing conservation areas
Leq (24) _ 50 dBA speech communication areas

Isolation provided if an impulsive sound exceed 10 dB above the baseline specification. No sound may exceed 30 dB above the baseline specification levels regardless of duration.

If acceptance level acoustic or vibration is performed to a minimum level which exceeds 6 dB down from the flight enveloped levels, the qualification levels must exceed the accewptance levels by 6 dB.

3.2.6 Transportability The RPC shall comply with NHB 6000.

3.3 Design and Construction

3.3.1 Parts, Materials, and Processes Parts, materials, and processes shall be selected and controlled in accordance with JSC 30233.

3.3.1.1 Electrical Connections Connections between wires shall be by positive, mechanically secure means such as crimped conductor splices, connectors, or terminal boards.

3.3.2 Electromagnetic Interference (EMI) The RPC shall meet the EMI requirments for Class A2 equipment specified in MIL-STD-461B.

3.3.2.1 Electrical Bonding Bonding shall be in accordance with MIL-B-5087.

3.2.5 Environmental Requirements The following structural and environmental dynamics requirements must be met for all components mounted internally to space station modules.

1) G. Ernsberger, "Guidelines for space station modules structural loads analysis", NASA MSFC memo ED22-85-40, 5 April 1986

2) NASA components analysis branch, "Design and verification guidelines for vibrocoustic and transient environments", NASA TM-86538, March 1986.

3) NASA/MSFC space station projects office, "Space Station Program Definition and Requirements" SS-SRD-0001, Sec. 30, 31 July 1986.

3.3.2.5 Electromagnetic Environment The RPC shall function normally during and after exposure to electromagnetic environment for class A2 equipment.

3.3.3 Nameplates and Product Markings

3.3.3.1 Identification Identification and marking of the RPC, its components, and parts shall be in accordance with MIL-STD-130. Nameplates shall be used, where applicable. Components within the RPC shall be identified by a part number and serial number assigned by the Supplier. Nameplates on the RPC shall include at least the following information:

Manufacturer's part number
Approved nomenclature - (from 1.1)
Controlling specification number - (from 1.2)
Manufacturer's name or trademark
Serial number - (Assigned by the Supplier as follows: The serial number shall consist of seven digits. The first three digits may be any combination of letters and digits provided the same combination is used for all part numbers. The last four digits shall be numeric and shall be assigned consecutively beginning with 0001. Serial numbers shall be non-repetitive.)
Contract number - (as specified in the Procurement Agreement)

3.3.3.1.1 Test Particles All Development RPC shall be permanently marked "Not for Operational Use - Development Only". All Operational type RPC which are subjected to qualification testing shall be permanently marked "Not for Operational Use - Qualification Only".

3.3.3.1.2 Equipment Labels Labels shall be engraved or chemically etched on the TBD surface, or engraved staked metal plates may be used. Paper decals and rubber stamping shall not be used. Identification sleeving may be used on electrical cables.

3.3.3.2 Electrical and Electronic Reference Designations Electrical and electronic reference designations for external electrical connectors shall be affixed to the RPC in accordance with the requirements of ANSI Y32.16 as modified by the Procurement Agreement.

3.3.4 Workmanship The RPC shall be fabricated and finished in a thoroughly workmanlike manner. Particular attention shall be given to freedom from blemishes, defects, burrs, and sharp edges; accuracy of dimensions; radii of fillets; marking of parts; thoroughness of cleaning; quality of brazing, welding, riveting, painting and wiring; alignment of parts; and tightness and torquing of fasteners.

3.3.5 Interchangeability and Replaceability Assemblies, components, and parts having identical part numbers shall, meet the requirements for an interchangeable item as defined in 6.1.4 herein. Where interchangeability is not practicable, the requirements for a replacement item as defined in 6.1.5 herein shall apply.

3.3.6 Safety. The design of the RPC shall be such that when the equipment is stored, transported, operated, or maintained in accordance with applicable precautions, it will not cause damage to itself or to other equipment, or cause injury to or be detrimental to the health of personnel. Hazardous conditions and or precautions to be observed shall be marked in a manner easily observed by personnel.

3.3.6.1 Pressure Vessels Pressure vessels shall be designed to "leak before burst" criteria and shall meet the design and qualification requirements of MIL-STD-1522.

3.3.7 Human Performance/Human Engineering

3.3.7.1 Crew Systems and Support Design of the RPC shall meet the requirements of MIL-STD-1472 and MSFC-STD-512.

3.3.7.3 Fasteners. Fasteners shall meet the requirements of MSFC-STD-512, section 4.4. Force related to fasteners shall comply to NASA RP1024.

3.3.7.4 Acoustical Noise Limits (See 3.2.5.3.1.5)

3.3.7.5 Surface Colors Surface colors shall be in accordance with FED-STD-595 and MSC SC-M-0003, and shall be subject to Martin Marietta approval.

3.3.8 Structural Integrity
(For definition of terms see Section 6)

3.3.8.1 Design The RPC shall be designed for the following design loads, limit load factors, and factors of safety:

3.3.8.1.1 Design Loads

3.3.8.1.2 Limit Load Factors

	Liftoff	Landing	
Vertical (Zo)	± 4.2	+8.2	+4.2
Longitudinal (Xo)	+ 2.5/-4.9	+3.6	
Side (Yo)	± 5.4	±7.2	

3.3.8.1.3 Factors of Safety (FS)

	General Structures
Yield FS	1.1
Proof FS	1.1
Ultimate FS	1.5

3.3.8.2 Margins of Safety All structures shall meet the requirement for zero or positive margins of safety calculated in accordance with SS-SRD-0001 Sec. 3.0, procedures.

3.3.8.3 Allowable Stresses The RPC shall be designed for material allowable stresses obtained as follows:

a. MIL-HDBK-5

b. Appropriate tests or sources approved by Martin Marietta.

The effects of temperature shall be accounted for in defining allowable material strength and properties.

3.3.8.4 Allowable Deflections The deflections of the RPC shall be designed such that there are no permanent deformations during normal operations.

3.3.9 Positive-locking Devices Positive-locking screw-type hardware shall be used on the RPC where practicable. Safety wiring shall be in accordance with MS33540.

3.3.11 Dimensioning and Tolerancing For figures herein dimensions are in millimeters. Dimensioning and tolerancing are per ANSI Y14.5. Unless otherwise specified, tolerances on mechanical features shall be as specified below:

Linear		X.XX	± .25
Angles	± 30 Minutes	X.X	± .75
		X 3	± 1
		X 3	± 2.5

3.3.12 Product Cleanliness Surfaces of hardware shall be free of all visible contamination, such as fingerprints, particles, corrosion products, metal chips, scale, oil, grease, preservatives, adhesives and any other foreign matter. Visual inspection shall be accomplished without magnification under good lighting conditions. Wipe tests, waterbreak tests, ultraviolet light inspection, special lights and mirrors, are considered aids to visual inspection.

Cleaned hardware shall be maintained in a clean area to prevent recontamination until such time that it is packaged in clean double bags for shipment.

External and internal surfaces shall meet the visually clean requirements described above. [Internal surfaces of fluid systems, i.e. valves, orifices, etc. are to be cleaned and verified to the individual requirements detailed by the design.]

The hardware shall be fabricated from materials that meet the material constraints of SP-R-0022A and cleaning procedures adequate to insure the removal of any process consumables used in the manufacture of the hardware shall be established.

3.3.13 Design for Test

3.3.13.1 System Partitioning The RPC shall be designed for compatibility with a partitioned fault detection/isolation system based upon the ability to confidently isolate faults. The ease or difficulty of fault isolation depends to a large extent upon the size and complexity of replaceable items. The following testability issues shall be considered for design partitioning:

3.3.13.1.1 Physical Partitioning The requirements for physical partitioning are as follows:

a. The maximum number of interface or interconnect points must be consistent with the interface capabilities of the proposed test equipment.

b. Where practical, components belonging to an inherently large ambiguity group should be placed in the same package.

c. Items should be limited to single design elements (such as only analog or only digital circuitry), whenever practical, and when functional partitioning is not impaired.

3.3.13.1.2 Functional Partitioning Whenever possible, each function should be implemented on a single replaceable item to make fault isolation straightforward. If more than one function is placed on a replaceable item, provisions should be made to allow for the independent testing of each function.

3.3.13.1.3 Block Partitioning Whenever possible, the item currently being tested should be isolated from items not being tested that are redundant or perform the same function. Provisions should be made for opening of feedback paths where practical.

3.3.13.2 Test Points Each item within the system shall have sufficient test points for the measurement or stimulus of internal nodes so as to achieve an inherently high level of fault detection and isolation. Test point selection shall be based upon the following:

a. Test points shall be readily accessible for connection to test equipment through system/equipment connections.

b. Test points shall be electrically decoupled from test equipment to assure that degradation of equipment performance does not occur as a result of connection to test equipment.

c. Test points shall be selected with due consideration for test equipment implementation and consistent with reasonable test equipment measurement accuracies and frequency requirements.

d. Test points shall be selected to segregate functional partitions.

e. Test points shall be chosen such that high voltage and current measurements are consistent with safety requirements and are physically isolated from low logic level signals.

f. Test point measurements shall relate to a common equipment ground.

3.3.13.6.1 Concurrent Concurrent (continuous) fault detection techniques (utilizing hardware redundancy) are used for monitoring those functions which are mission critical or affect safety and where protection must be provided against the propagation of errors through the system.

3.3.13.6.2 Periodic Periodic testing is used for monitoring those functions which provide backup or standby capabilities or are not mission critical.

3.3.13.6.3 On-demand On-demand testing is used for monitoring those functions which require operator interaction, sensor simulation, or which are not easily, safely, or cost-effectively initiated automatically.

3.3.13.6.4 Maintenance Capability For each level of maintenance, Built-in-test (BIT), off-line automatic test and manual test capabilities shall be integrated to provide a consistent and complete maintenance capability. The degree of test automation shall be consistent with the proposed personnel skill levels and corrective and preventive maintenance requirements.

3.4 Supplier Documentation The Supplier shall furnish documentation in accordance with the Procurement Agreement.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General This section describes the requirements for the verification of the Section 3 requirements during design and fabrication, and acceptance and qualification test programs.

4.1.1 Responsibility for Verification The Supplier shall perform all or any part of the verification activities of this drawing when so required by Martin Marietta in the Procurement Agreement. In the event Martin Marietta elects to perform any part or all of the tests identified, or have them performed by others, the Supplier shall either write the test procedures or comment and mutually agree upon the test procedures. The direction for either originating or approving these test procedures will be in the Procurement Agreement. The Supplier shall either provide technical direction or shall have representation present for any part or all of the tests when required by the Procurement Agreement. The Supplier may monitor these tasks at his option and shall accept the results of any tests which have been performed in accordance with procedures approved by the Supplier. The Supplier shall accept the results whether Martin Marietta or the Supplier contracts for the testing.

4.1.2 Quality Assurance Requirements A Quality Assurance Program shall be conducted at the supplier's facilities in accordance with the quality assurance requirements defined in the Procurement Agreement.

4.1.3 Notification of Tests The Martin Marietta buyer shall be notified 10 days prior to the time tests are to be conducted. In addition, Martin Marietta reserves the right to witness all tests.

4.1.4 Test Program Controls The Supplier shall incorporate the following test program controls.

4.1.4.1 Facilities and Equipment Facility and equipment requirements shall be as specified in M-67-45 Sections 4 and 5. In addition, still and video photographs shall be required to the extent defined in the Procurement Agreement.

4.1.4.2 Non-conformance Reporting Non-conformance reporting shall be as specified in M-67-45 Section 9..

4.1.4.3 Test Documentation Test documentation shall be prepared in accordance with M-67-45 Section 6.

4.1.4.4 Test Methods and Conditions Implementation of the test requirements herein shall be in accordance with the detailed test methods and conditions specified in M-67-45. Requests for any deviations from M-67-45 deemed necessary shall be approved by Martin Marietta. The test procedure shall be prepared by the Supplier and approved by Martin Marietta in writing prior to the start of any tests.

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4.2 Quality Conformance Verification - The requirements of Section 3 herein shall be verified by combination of inspection, demonstration, analysis and testing. Table I defines the verification requirements that shall be used to satisfy the requirements specified in Section 3. In addition, functional and performance tests shall be conducted in the testing sequence (Tables II and III) to evaluate the effects of testing.

4.2.1 Verification Methods The following methods shall be used:

a. Inspection Inspection is a method of verification consisting of investigation, without the use of special laboratory appliances or procedures, to determine compliance with requirements. Inspection is nondestructive and includes (but is not limited to) visual examination, simple physical manipulation, gauging, and measurement.

b. Demonstration Demonstration is a method of verification that is limited to readily observable functional operation to determine compliance with requirements. This method may not require the use of special equipment or sophisticated instrumentation.

c. Analysis Analysis is a method of verification taking the form of the processing of accumulated results and conclusions, intended to provide proof that verification of a requirement or requirements has been accomplished. The analytical results may be based on engineering study, compilation or interpretation of existing information, similarity to previously verified requirements, or derived from lower level examinations, tests, demonstrations, or analyses. Submittal of analysis data shall be as required in the Procurement Agreement.

d. Test Test is a method of verification that employs technical means including (but not limited to) the evaluation of functional characteristics by use of special equipment or instrumentation, simulation techniques, and the application of established principles and procedures to determine compliance with requirements.

4.2.1.1 Qualification by Similarity When qualification by similarity to a previously qualified item is proposed by the supplier such qualifications shall be subject to Martin Marietta approval and shall meet the requirements specified in the Procurement Agreement.

4.2.2 Test Category Definitions

a. Development Tests Development testing is a test or series of tests conducted to evaluate and confirm the feasibility of the design approach and provide confidence in the ability of the hardware to meet qualification and acceptance requirements. Tests shall be performed primarily to acquire data to support the design and development process. The development hardware should be representative of, but not necessarily identical to, production hardware.

b. Acceptance Tests Acceptance tests are the required formal tests conducted to demonstrate acceptability of an item for delivery. Acceptance tests may consist of performance, functional and acceptance level environmental tests. This testing is conducted to detect manufacturing flaws and defects that may not be detected by other inspection techniques. Acceptance tests shall be performed on each production and qualification unit.

c. Qualification Tests Qualification (certification) tests are formal contractual demonstrations that the design, implementation, and manufacturing methods have resulted in hardware conforming to specification requirements. The qualification tests are usually conducted at levels and for durations that assure the production items will perform satisfactorily in the use environments with sufficient margin. Qualification hardware is fabricated to production equipment drawings using specified materials and production methods and shall be representative of deliverable production hardware. Qualification testing shall be conducted as part of the total verification process of the design and fabrication compliance.

4.2.3 Test Type

a. Performance Test The operating test that verifies all functions and circuits are operating as required by the unit design specification. All performance tests may be conducted at laboratory ambient conditions. Performance tests shall be conducted at the start and conclusion of the acceptance and qualification test program.

b. Functional Test The operating test that is normally a subset of the performance test requiring minimal operation to verify proper operation of the unit under test. These tests shall be conducted before, during, and after each environmental test as defined herein. Functional tests shall be performed at laboratory ambient conditions or the environmental exposure conditions when specified.

4.3 Test Requirements

4.3.1 Development Tests Development testing shall be performed only when specified in the procurement agreement. Any development testing that is not specified in the Procurement Agreement shall be the sole responsibility of the Supplier. The results of such tests will not be accepted by Martin Marietta for design verification purposes. The results of any development tests specified in the Procurement Agreement shall be documented and submitted to

Martin Marietta for Engineering concurrence. In the event such specified development test results are intended to be used as part of the verification process, the test shall be predeclared and the test controls specified in the Procurement Agreement shall be applied.

4.3.2 Acceptance Tests - Acceptance tests as specified in Tables I and II shall be conducted on each production unit and each qualification test unit. Performance and acceptance testing of items requiring computer control shall be performed with validated computer control software or a Martin Marietta approved simulation thereof. Operation with computer control acceptable to Martin Marietta shall be a condition of acceptance testing.

4.3.2.1 Performance Tests Tests shall be conducted to verify or support verification with Paragraphs 3.2, 3.2.6, and 3.3. The sequence of testing shall be as listed in Table II in accordance with paragraph 4.2.3, herein.

4.3.2.2 Functional Tests Functional tests shall be performed to demonstrate compliance with paragraphs 3.2 and 3.3. The order of testing the functional parameters shall be as listed in Table II. These tests shall be conducted before, [during], and after each environmental test as defined in 4.3.2.3 and subparagraphs.

4.3.2.3 Environmental Tests Performance test, as defined in 4.2.3 shall be conducted prior to the first environmental test and after completion of all environmental tests. [PD Writer; List all the acceptance environmental tests that are required to be performed in sequence, i.e., examples below: If sequence is a problem, consult the System Test Group.] Tests shall be performed in the sequence shown in Table II.

4.3.2.3.1 Acceptance Thermal Vacuum Test Components (subassemblies) identified as sensitive to a vacuum environment shall be tested in accordance with Paragraph 8.3 of M-67-45, with the temperature limits and durations noted below.

4.3.2.3.1.1 Acceptance Temperature Limits The 10°C qualification margin shall be subtracted from the maximum and minimum qualification limits defined in para. 3.2.5.1.1 herein.

4.3.2.3.1.2 Acceptance Test Duration - A minimum of 8 thermal vacuum cycles are required. The dwell times at maximum and minimum temperatures shall be a minimum of 2 hours after temperature stabilization except that a 12 hour dwell after temperature stabilization with a cold start shall be required in the first cycle and a 12 hour hot dwell after temperature stabilization with a hot start shall be required in the last cycle.

4.3.2.3.1.3 Stabilization of Test Temperature The test unit and baseplate/chamber temperatures shall be stabilized prior to the start of the test. Temperature stabilization shall be considered established when the readings of all central temperature sensing devices are within 1.7°C (3°F) of the specified temperature for 3 consecutive readings taken 5 minutes

apart. For test units larger than 13.6 kg (30 pounds), stabilization shall be considered established when 3 consecutive readings taken 5 minutes apart are within 2.8°C (5°F) of the specified temperature. During thermal cycling, chamber temperatures shall be measured using a minimum of two temperature sensing devices located in the free airflow, within 12.7 cm of opposite sides of the test unit. Baseplate temperatures shall be measured using a minimum of 2 temperature sensing devices located at opposite sides of the thermal interface. Temperature of the test unit shall be measured using a minimum of 2 temperature sensing devices located as near as possible to the mass center of the test unit. During thermal vacuum testing, temperature sensing devices shall be placed on all chamber walls and doors as well as the baseplate to verify stabilization. Application of temperature stabilization shall be in accordance with Paragraph 8.3 (thermal vacuum) and 8.4 (thermal cycling) of M-67-45.

4.3.2.3.2 Acceptance Thermal Cycle Test The RPC shall be tested in accordance with Paragraph 8.4 of M-67-45 with the temperature limit and duration exception noted below. Functional testing shall be limited to a pre and post test functional test plus periodic abbreviated functional tests during the thermal cycling test to verify performance.

4.3.2.3.2.1 Temperature Limits The 10°C qualification margin shall be subtracted from the maximum and minimum qualification limits defined in para.3.2.5.1.1 herein. The stabilization requirements of paragraph 4.3.2.3.1.3 also apply to this test.

4.3.2.3.2.2 Test Duration A minimum of 8 thermal cycles are required on components not thermal vacuum tested. For component level acceptance tests, thermal vacuum or thermal cycle tests are required, but not both. For thermal cycle tests the dwell times at maximum and minimum temperatures shall be a minimum of 2 hours after temperature stabilization except that a 12 hour cold dwell after temperature stabilization with a cold start shall be required in the first cycle and a 12 hour hot dwell after temperature stabilization with a hot start shall be required in the last cycle.

4.3.2.3.4 Acceptance Random Vibration The RPC shall be tested in accordance with Paragraph 8.21 of M-67-45 except that the test levels shall be those specified by Martin Marietta. The duration of the acceptance random vibration test shall consist of a 1.0 minute exposure in each of the three orthogonal axis. A functional test shall be performed prior to and after completion of testing in all three axes. Power spectral density plots of the input acceleration and cross-axes response shall be provided.

4.3.2.3.5 Acceptance Pressure/Leak Test The RPC shall be acceptance tested for pressure and leakage in accordance with the respective Paragraphs 8.12 and 8.11 of M-67-45. Batteries shall be tested at the cell level only.

4.3.2.3.6 Acceptance Weight Measurement After completion of the acceptance level environmental tests, a weight measurement test shall be performed on the unit. The weight of the unit shall be measured in a condition nearly equivalent to the launch manifest configuration. The equipment status at the time of measurement shall be logged and shall become a part of the records and weight report.

4.3.2.3.7 Acceptance Run-in-Test Mechanical and electromechanical components and subassemblies shall be mechanically cycled in accordance with Paragraph 8.37 of M-67-45.

4.3.3 Qualification Tests - Qualification tests shall be performed on each test unit as specified in Tables I and III. Test articles shall be the same configuration as the production hardware. Successful completion of inspections and acceptance tests of Section 4 shall be a prerequisite to each test unit entering qualification test.

4.3.3.1 Performance Tests The same test conditions specified in paragraph 4.3.2.1 shall apply using the test sequence listed in Table III. With Martin Marietta approval, the final acceptance performance test may serve as the pre-qualification performance test.

4.3.3.2 Functional Tests Functional tests shall be performed to demonstrate compliance with paragraphs 3.2.1, and 3.3.2. The order of testing the functional parameters shall be as listed in Tables I and III. These tests shall be conducted before, [during], and after each environmental test as defined in 4.3.3.3 and subparagraphs.

4.3.3.3 Environmental tests Environmental tests shall be performed in the sequence shown in Table III.

4.3.3.3.1 Qualification Thermal Vacuum Test Components identified as sensitive to a vacuum environment shall be tested in accordance with Paragraph 8.3 of M-67-45. With the temperature limits and durations noted below.

4.3.3.3.1.1 Qualification Test Temperature Limits Test temperature limits are determined by the type of thermal control system employed.

a. Passive Thermal Control The maximum predicted plus 21°C and the minimum predicted minus 21°C.

b. Active Thermal Control (applicable to coldplate mounted items) The maximum predicted plus 21°C and the minimum predicted minus 10°C.

4.3.3.3.1.2 Qualification Test Durations A minimum of 8 thermal vacuum cycles are required on vacuum sensitive components. The dwell times at maximum and minimum temperatures shall be a minimum of 2 hours after temperature stabilization except that a 12 hour cold dwell after temperature stabilization with a cold start shall be required in the first cycle and a 12 hour hot dwell after temperature stabilization with a hot start shall be required in the last cycle.

4.3.3.3.1.3 Stabilization of Qualification Test Temperature The test unit and baseplate/chamber temperature shall be stabilized prior to the start of the test. Temperature stabilization shall be considered established when the readings of all central temperature sensing devices are within 1.7°C (3°F) of the specified temperature for 3 consecutive readings taken 5 minutes apart. For test units larger than 13.6 kg (30 pounds), stabilization shall be considered established when 3 consecutive readings taken 5 minutes apart are within 2.8°C (5°F) of the specified temperature. During thermal cycling, chamber temperatures shall be measured using a minimum of two temperature sensing devices located in the free airflow, within 12.7 cm of opposite sides of the test unit. Baseplate temperatures shall be measured using a minimum of 2 temperature sensing devices located at opposite sides of the thermal interface. Temperature of the test unit shall be measured using a minimum of 2 temperature sensing devices located as near as possible to the mass center of the test unit. During thermal vacuum testing, temperature sensing devices shall be placed on all chamber walls and doors as well as the baseplate to verify stabilization. Application of temperature stabilization shall be in accordance with Paragraph 8.3 (thermal vacuum) and 8.4 (thermal cycling) of M-67-45.

4.3.3.3.2 Qualification Thermal Cycle Test Components shall be tested in accordance with Paragraph 8.4 of M-67-45 with the temperature limits and durations noted below. Periodic abbreviated functional testing shall be performed during thermal cycling test to verify performance.

4.3.3.3.2.1 Qualification Temperature Limits Same as for thermal vacuum in Paragraph 4.3.3.3.1.1 herein.

4.3.3.3.2.2 Qualification Test Durations

4.3.3.3.2.2.1 Vacuum Sensitive Components Components which have been thermal vacuum tested will not be thermal cycled.

4.3.3.3.2.2.2 Components Not Vacuum Sensitive Components that are not thermal vacuum tested will be exposed to 8 thermal cycles. The dwell times at maximum and minimum temperatures shall be a minimum of 2 hours after temperature stabilization except that a 12 hour cold dwell after temperature stabilization with a cold start shall be required in the first cycle and a 12 hour hot dwell after temperature stabilization with a hot start shall be required in the last cycle.

4.3.3.3.3 Qualification Random Vibration Components (subassemblies) shall be tested in accordance with Paragraph 8.21 of M-67-45. The test levels shall be specified by Martin Marietta. The duration of the random vibration test shall consist of 3.0 minute exposure in each of the three orthogonal axis. During the test, the components shall be attached to a rigid test fixture representative of its mounting. A functional test shall be performed prior to and after completion of testing in all three axes. Power spectral density plots of the input acceleration and cross-axis response shall be provided.

4.3.3.3.4 Qualification Acceleration Test

4.3.3.3.5 Qualification Pressure/Leak Test As applicable, components shall be tested in accordance with Paragraphs 8.12 and 8.11 of M-67-45 for pressure and leak tests respectively. Batteries shall be tested at the cell level only.

4.3.3.3.6 Qualification EMC Test The electromagnetic interference characteristics (emission and susceptibility) of the components (subassemblies) shall be tested in accordance with Paragraph 8.35 of M-67-45.

4.3.3.3.7 Life Test Life testing shall be as specified in Paragraph 8.36 of M-67-45.

4.3.3.3.8 Toxicity Tests The RPC shall be tested as specified in TBS.

4.3.3.3.9 Audible Noise Measurements The RPC shall be tested for emitted audible noise as specified in TBS.

4.3.4 Certification The hardware represented by this document shall be certified relative to the Section 3.0 requirements herein. The supplier shall provide documentation to support certification as specified in the Procurement Agreement.

5.0 PREPARATION FOR DELIVERY

5.1 General Preparation for delivery shall be in accordance with the terms of the Procurement Agreement.

5.2 Marking For Shipment Marking for shipment shall be in accordance with MIL-STD-129.

6.0 NOTES

6.1 Definitions

6.1.1 Supplier The Supplier is the organization awarded the Procurement Agreement.

6.1.2 Procuring Agency The Procuring Agency is Martin Marietta Denver Aerospace or as designated in the Procurement Agreement.

6.1.3 Procurement Agreement The Procurement Agreement is the written purchase order, subcontract, or other instrument of purchase or intent to purchase, as agreed by Martin Marietta and the Supplier, including any written negotiated changes or revisions thereto. The Procurement Agreement will supplement the following paragraphs of this Drawing.

2.1	Applicable Document Revision Letter or Date
3.3.3.1	Identification
3.3.3.2	Electrical and electronic reference designations
3.4	Supplier Documentation
4.1.1	Responsibility for Tests
4.1.2	Quality Assurance Requirements
4.1.4.1	Facilities and Equipment
4.2.1.c	Analysis
4.2.1.1	Qualification by Similarity
4.3.1	Development Tests
5.1	Preparation for Delivery

6.1.4 Interchangeable Items When two or more items possess such functional and physical characteristics as to be equivalent in performance and durability and are capable of being exchanged one for the other without alteration of the items themselves or of adjoining items except for adjustment, and without selection for fit or performance, the items are interchangeable. Interchangeable items are manufactured with the aid of controlled tooling and require only the application of attaching means for their installation.

6.1.5 Replaceable Item An item which is functionally interchangeable with another item, but which differs physically from the original part in that the installation of the replaceable part requires operations such as drilling, reaming, cutting, filing, shimming, etc., in addition to the normal applications and methods of attachment, is known as a replaceable item. Replaceable items are manufactured with the aid of controlled tooling and require alteration of the items in addition to normal methods of attachment.

6.1.6 Part One piece or two or more pieces joined together which are not normally subject to disassembly without destruction of designed use.

6.1.7 Component A combination of parts, devices and structures, usually self-contained, which performs a distinctive function in the operation of the overall equipment, e.g., a "black box".

6.1.8 Operating Failure Rate The operating failure rate represents a mathematical combination of failure rates associated with a part's failure modes which might occur in an operational sequence. The operating failure rate is analytically determined.

6.1.9 Launch Manifest Configuration TBS.

6.1.10 Limit Factors A load factor is a ratio by which the mass of an assembly or an external load, is multiplied in order to obtain the limit load action on the structure or a part thereof.

6.1.11 Limit Load Limit load is the maximum load or force expected in service for a particular design condition and includes the effects of dynamics.

6.1.12 Yield Load The yield load is equal to the limit load multiplied by the yield factor of safety. The yield load is that load at or below which general yielding of the structure must not occur.

6.1.13 Ultimate Load The ultimate load is equal to the limit load multiplied by the ultimate factor of safety. Rupture or complete structural collapse shall not occur at or below ultimate load.

6.1.14 Proof Load The proof load is equal to the limit load multiplied by the proof safety factor. The proof load shall be of sufficient magnitude to assure that the part can sustain limit load conditions, as required, throughout its service life.

6.1.15 Factor of Safety The factor of safety is an arbitrary factor intended to account for slight variation from item to item in fabrication quality and details, internal load distribution within the structure and possible degradation in strength.

6.1.15.1 Yield Factor of Safety The yield factor of safety is the ratio of yield to limit load.

6.1.15.2 Ultimate Factor of Safety The ultimate factor of safety is the ratio of ultimate load to limit load.

6.1.15.3 Proof Factor of Safety The proof factor of safety is the ratio of proof load to limit load.

6.1.16 Yield Strength Yield strength (stress) is the stress at which a structural material exhibits a 0.2 percent permanent deformation.

6.1.17 Ultimate Strength Ultimate strength (stress) is the maximum stress which a structural material exhibits prior to material rupture or other failure mechanism of the material.

6.1.18 Orbital Replaceable Unit (ORU) Orbital Replaceable units are hardware elements whose design enables Remote Automatic fault detection/fault isolation, removal, replacement and checkout by organizational maintenance.

6.1.19 Circuit Isolation The intercircuit isolation requirement applies between functional electrical circuits which interface between two equipments. The requirement applies over the operating frequency range of the circuits.

6.1.20 Electrical Circuit Reference Connection For the purpose of the circuit to reference connection requirement, an electrical circuit is defined as a functional electrical connection between two equipments.

6.1.21 Electrical Reference All conductive parts which are not part of functional electrical circuits are bonded together to form an electrical reference. The electrical reference is not used for the conduction of functional current, except for vehicle lighting.

6.2 Abbreviations and Acronyms Unless otherwise defined, abbreviations are in accordance with MIL-STD-12 and acronyms are as follows:

EM	- Electromagnetic
EMI	- Electromagnetic Interference
EMP	- Electromagnetic Pulse
FS	- Factor of Safety
MTBF	- Mean Time Between Failure
MTTR	- Mean Time To Repair
ORU	- Orbit Replaceable Unit
PM&P	- Parts, Materials, and Processes
RFP	- Request For Proposal
TBD	- To Be Determined by Supplier
TBS	- To Be Supplied by Martin Marietta

6.3 Deviations Deviations to this Drawing will be allowed only be written authorization from Martin Marietta followed by a revision to this Drawing.

6.4 Authorized Representative No representative of Martin Marietta other than the assigned buyer or his superiors will be empowered to make any commitments for Martin Marietta.

6.5 Correspondence and Data All correspondence regarding requirements set forth herein is to be addressed to Martin Marietta, attention of the assigned buyer. All data is to be similarly addressed.

SERIAL DATA FORMAT

BIT	SWITCHED ON	SWITCHED TRIPPED
15 (MSB)	SWITCH ON (3)	SWITCH ON (3)
14	SELF-TEST (2)	SELF-TEST (2)
13	SEQ. DATA 2 (4)	SPARE
12	SEQ. DATA 1 (4)	SPARE
11	OVER-TEMPERATURE (present)	OVER-TEMPERATURE (prsent)
10	SPARE	SPARE
9	SPARE	SPARE
8	CURENT OVER-RANGE	OVER TEMPERATURE (1 atch)
7	CURRENT (MSB)	TRIPPED/GROUND FAULT
6	CURRENT	TRIPPED/UNDERVOLTAGE
5	CURRENT	TRIPPED/OVERCURRENT
4	CURRENT	SPARE
3	CURRENT	SPARE
2	CURRENT	SPARE
1	CURRENT (LSB)	SPARE
0 (LSB)	PARITY (ODD)	PARITY (ODD)

NOTES: (1) Set to "1" when current is ___ 100%.
(2) Set to "1" when switch fails internal self-test.
(3) Set to "1" when switch is not tripped.

TABLE 5

RPC RATINGS

Item	Current Rating	Overload (1) Trip (Min)	Fault (2) Trip (Max)	Initial Turn-On Current	Max On-State Power Diss.
1	2.5 A	2.75A	10.75A	5.62±.625 A	5 W
2	5 A	5.5 A	21.5 A	11.25±1.25 A	10 W
3	15 A	16.5 A	64.5 A	33.75±3.75 A	30 W
4	25 A	27.5 A	107.5 A	56.25±6.25 A	50 W

(1) Refer to Fig. 1
(2) SMS Max.

TABLE 6

TABLE I

VERIFICATION REQUIREMENTS CHECK LIST

DESIGN REQUIREMENTS NOTE: PARAGRAPH REFERENCE INCLUDES SUBPARAGRAPHS.	VERIFICATION METHOD						TEST REQUIREMENTS NOTE: PARAGRAPH REFERENCE INCLUDES SUBPARAGRAPHS
	ANALYSIS	DEMONSTRATION	INSPECTION	DEVELOPMENT TEST	ACCEPTANCE TEST	QUALIFICATION TEST	
3 REQUIREMENTS							TITLE
3.1 ITEM DEFINITION							NO VERIFICATION ITEM
3.2 CHARACTERISTICS		X			X	X	4.2.1B, 4.3.2, 4.3.3
3.2.1 PERFORMANCE CHAR.S				X		X	4.3.2, 4.3.3
3.2.1.1 POWER					X		4.3.2
3.2.1.1.1 POWER INPUT							TITLE
3.2.1.1.1.1 POWER CONSUMPTION					X		4.3.2
3.2.1.2 POWER SWITCH		X			X		4.2.1b, 4.3.2
3.2.1.3 TRIP CHARACTERISTICS		X			X		4.2.1b, 4.3.2
3.2.1.3.1 OVERLOAD							
3.2.1.3.2 INITIAL TURN-ON							
3.2.1.3.3 LOAD FAULTS							
3.2.1.3.4 RESET							
3.2.1.3.5 GROUND FAULT							
3.2.1.3.6 POWER SUPPLY SURGES							
3.2.1.3.7 POWER SUPPLY BLACKOUT							
3.2.1.4 CONTROL CIRCUITS		X			X		4.2.1b, 4.3.2
3.2.1.4.1 LOGIC LEVELS							
3.2.1.4.1 ON/OFF CONTROL INPUT							
3.2.1.4.4 DATA ENABLE							
3.2.1.4.5 CLOCK							
3.2.1.4.6 SMART CONTACTOR ENABLE							
3.2.1.4.7 LOAD ISOLATION/CONTACT							
OR COIL DRIVE AND POSITION							
3.2 .1.5 MONITOR CIRCUITS		X			X		4.2.1b, 4.3.2

TABLE I

VERIFICATION REQUIREMENTS CHECK LIST

DESIGN REQUIREMENTS NOTE: PARAGRAPH REFERENCE INCLUDES SUBPARAGRAPHS.	VERIFICATION METHOD						TEST REQUIREMENTS NOTE: PARAGRAPH REFERENCE INCLUDES SUBPARAGRAPHS
	ANALYSIS	DEMONSTRATION	INSPECTION	DEVELOPMENT TEST	ACCEPTANCE TEST	QUALIFICATION TEST	
3.2.1.5.1 LOGIC LEVELS							
3.2.1.5.2 STATUS DISCRETE		X			X		4.2.1b, 4.3.2
3.2.1.6 RPC LOADS			X				4.2.1a
3.2.2 PYSICAL CHARACTERISTICS			X				4.2.1a
3.2.3 RELIABILITY			X				4.2.1a
3.2.4 MAINTAINABILITY							
3.2.5 ENVIRONMENTS REQUIREMENT							
3.2.5.1 GROUND STORAGE							
TRANSPORTATION AND HANDLING							
3.2.5.2 GROUND OPERATION ENVIR.							
3.2.5.3 LAUNCH AND DESCENT ENVIR.							
3.2.5.4 ORBITAL OPERATION ENVIR.			X		X		4.2.1a, 4.3.2
3.2.6 TRANSPORTABILITY			X		X		4.2.1a, 4.3.2
3.3 DESIGN AND CONSTRUCTION							
3.3.2 ELECTROMAGNETIC		X		X		X	4.2.1b ,4.3.1, 4.3.3
INTERFERENCE (EMI)							
3.3.3 NAMEPLATES AND PRODUCT							
MARKINGS							
3.3.4 WORKMANSHIP							
3.3.5 INTERCHANGEABILITY AND							
REPLACEABLILITY		X					4.2.1b
3.3.6 SAFETY							
3.3.7 HUMAND PERFORMANCE/		X					4.2.1b
HUMAN ENGINEERING							
.3.3.8 STRUCTURAL INTEGRITY							

TABLE I

VERIFICATION REQUIREMENTS CHECK LIST

DESIGN REQUIREMENTS NOTE: PARAGRAPH REFERENCE INCLUDES SUBPARAGRAPHS.	VERIFICATION METHOD						TEST REQUIREMENTS NOTE: PARAGRAPH REFERENCE INCLUDES SUBPARAGRAPHS
	ANALYSIS	DEMONSTRATION	INSPECTION	DEVELOPMENT TEST	ACCEPTANCE TEST	QUALIFICATION TEST	
3.3.9 POSITIVE - LOCKING DEVICES							
3.3.11 DIMENSIONING AND TOLERANCE							
3.3.12 PRODUCT CLEANLINESS							
3.3.13 DESIGN FOR TEST							

TABLE II ACCEPTANCE			
PERFERRED TEST SEQUENCE	SECTION 3	SECTION 4	TEST CONDITIONS/REMARKS
PERFORMANCE	3.2.1	4.3.2.1	
FUNCTIONAL		4.3.2.2	
ENIRONMENTAL		4.3.2.3	
FUNCTIONAL		4.3.2.2	
THERMAL VACUUN		4.3.2.3.1	
FUNCTIONAL		4.3.2.2	
RANDOM VIBRATION		4.3.2.3.4	
FUNCTIONAL		4.3.2.2	
FRESSURE/LEAK		4.3.2.3.5	
WEIGHT MEASUREMENT		4.3.2.3.6	
RUN - IN - TEST		4.3.2.3.7	
PERFORMANCE		4.3.2.1	

TABLE III QUALIFICATION TESTS

PERFERRED TEST SEQUENCE	SECTION 3	SECTION 4	TEST CONDITIONS/REMARKS
ACCEPTANCE		4.3.2	
FUNCTIONAL		4.3.3.2	
THERMAL CYCLE		4.3.3.3.2	
FUNCTIONAL		4.3.3.2	
RANDOM VIBRATION		4.3.3.3.3	
FUNCTIONAL		4.3.3.2	
ACCELERATION		4.3.3.3.5	
FUNCTIONAL		4.3.3.2	
EMC		4.3.3.3.7	
FUNCTIONAL		4.3.3.2	
AUDIBLE NOISE		4.3.3.10	
FUNCTIONAL		4.3.3.2	
SALT FOG			
FUNCTIONAL			
PRESSURE/LEAK			
FUNCTIONAL			
PERFORMANCE			

TABLE IV DESIGN DEVELOPMENT TESTS

PERFERRED TEST SEQUENCE	SECTION 3	SECTION 4	TEST CONDITIONS/REMARKS
PREFORMANCE CHARICTRISTICS AND SUBPARAGRAPHS.	3.2.1	4.3.1	
ELECTROMAGNETIC INTERFERNCE (EMI)	3.3.2	4.3.1	

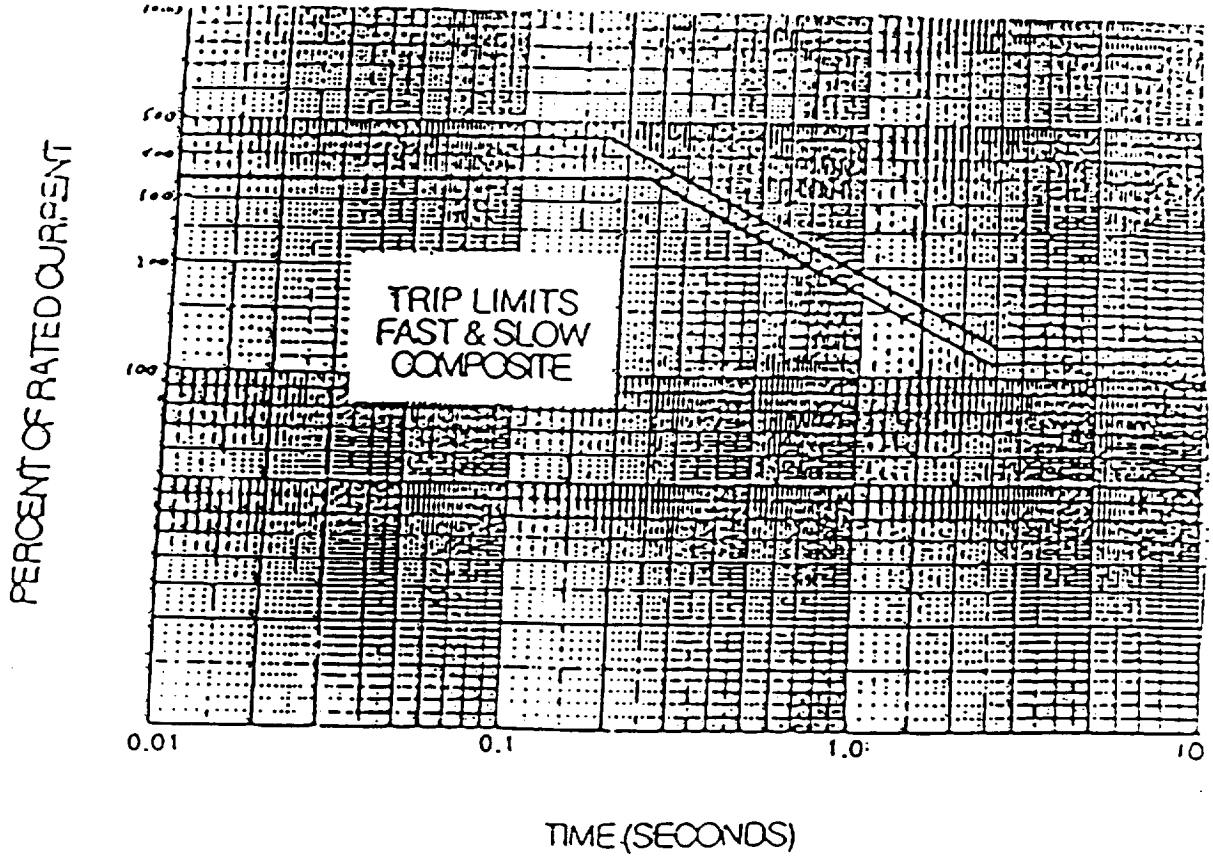


FIGURE 1. RPC TRIP CHARACTERISTICS

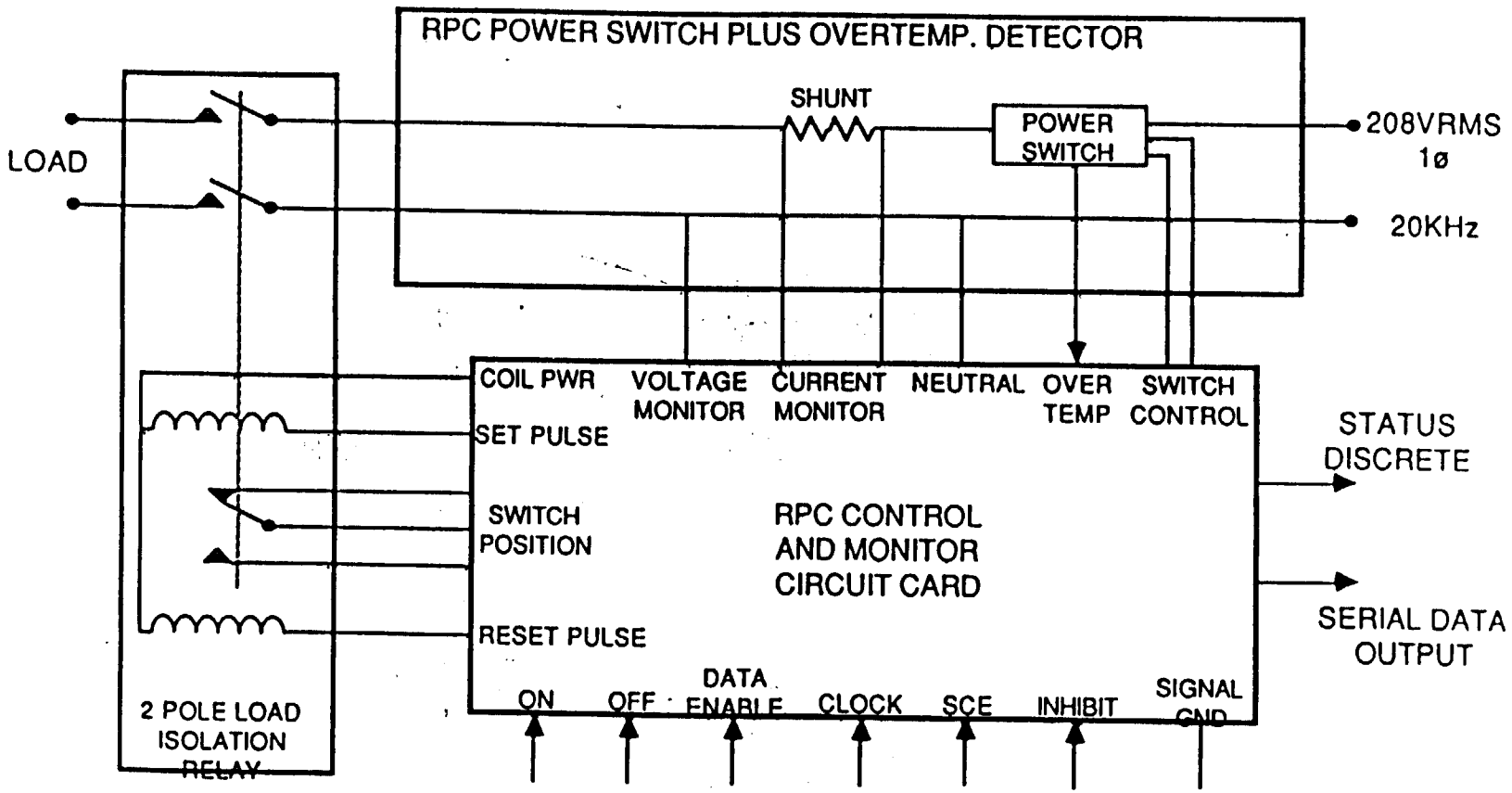


FIGURE 2. RPC CONFIGURED WITH LOAD ISOLATION RELAY

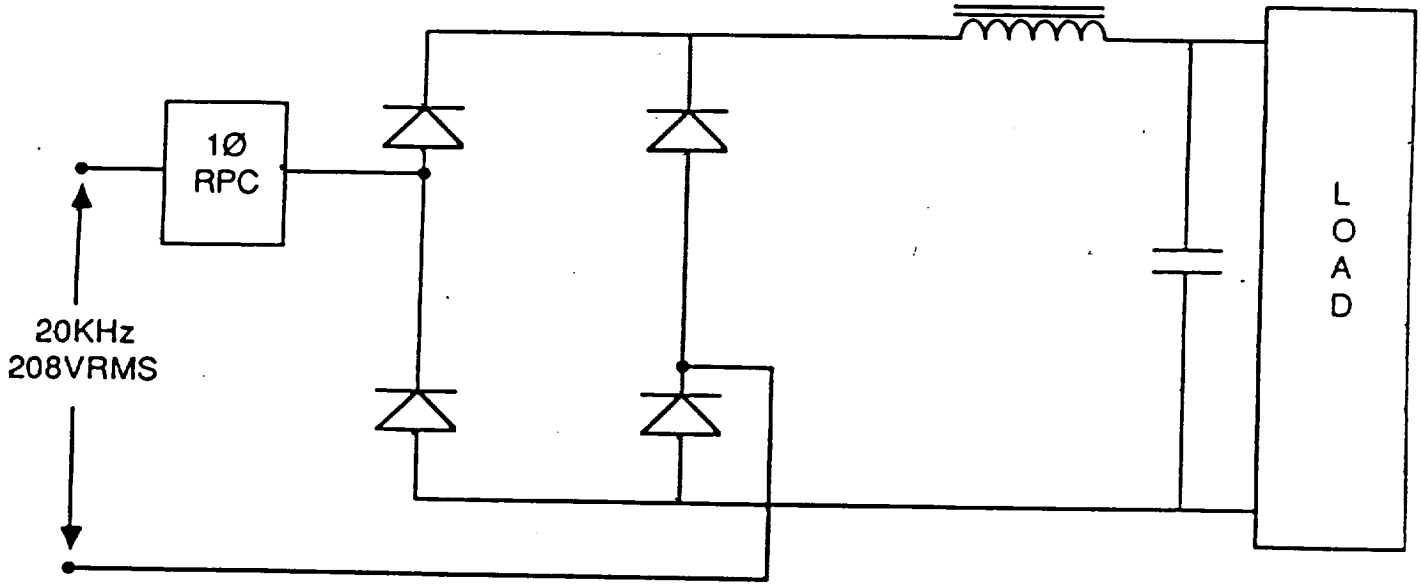
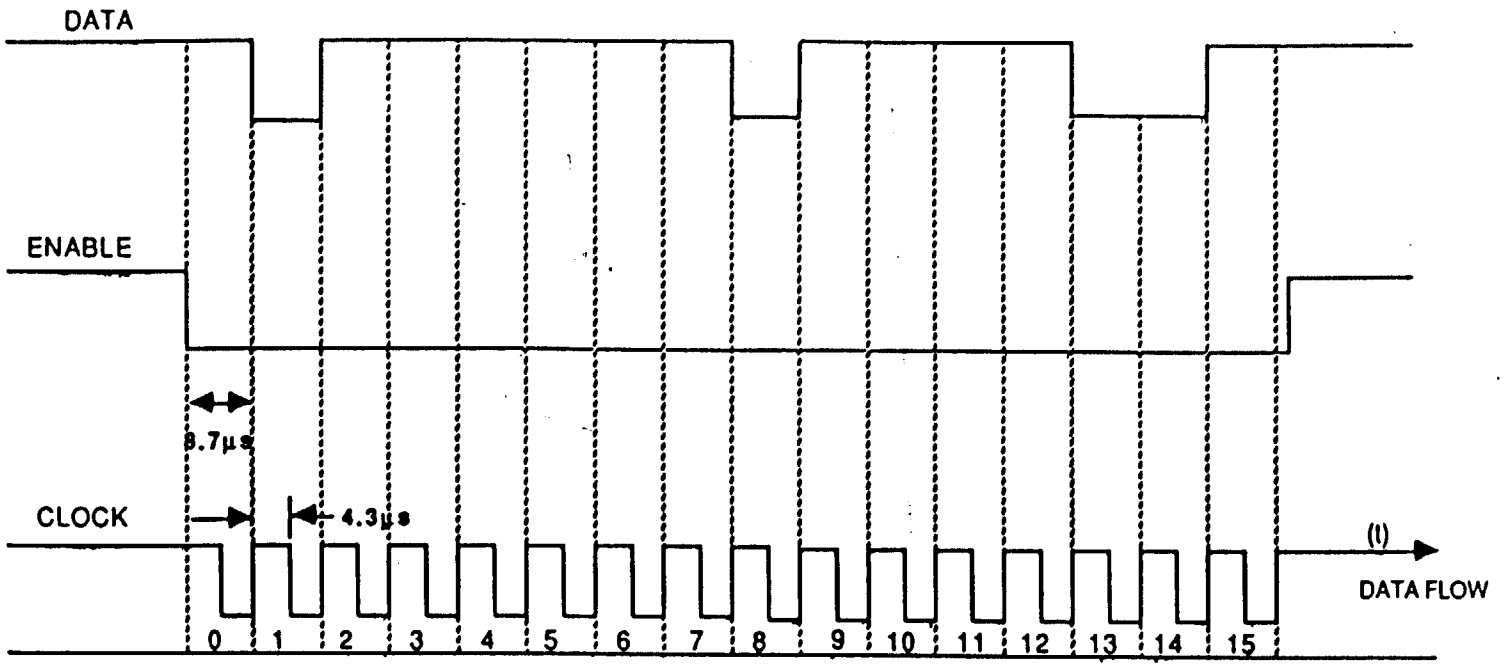


FIGURE 4. OFFLINE BRIDGE LOADING OF RPC



SINGLE PHASE RPC (5A RPC)

NOTES;

1) IDEALIZED WAVEFORMS DEPICTED

2) TIMING IS NOMINAL WITH TOLERANCE = +/-5%

3) DATA BITS SHALL BE STABLE ON DATA SOURCE OUTPUT LINE MORE THAN 1.75µsec PRIOR TO EACH FALLING EDGE OF THE CLOCK.

4) DATA HOLD TIME = Tdm = 0

5) SERIAL DATA FORMAT SHOWN IN TABLE1.

FIGURE 5. RPC SERIAL DATA TIMING DIAGRAM

APPENDIX IV

10 kW DC Remote Controlled Circuit Breaker (RCCB) Product Control Drawing

This product control drawing was developed for Martin Marietta by Teledyne Solid State Products. This document provides basic specifications for the DC RCCB power stage.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON MODEL NO.	REV.	DESCRIPTION	DATE	APPROVED
	ICF0010-09C	1	PRELIM RLSE ECN 14734	9/8/87	

PRELIMINARY
RELEASE

ORIGINAL PAGE IS
OF POOR QUALITY

PRODUCT CONTROL DRAWING
(P.C.D.)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ± .
.XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.		
	APPROVALS	DATE
DRAWN	A.POMAR	8-19-87
CHECKED		8-24-87
ENGINEER		8-25-87

TELEDYNE SOLID STATE PRODUCTS
HAWTHORNE, CALIFORNIA

67 AMP REMOTE POWER CONTROLLER

SIZE	FSCM NO.	DWG. NO.	REV.
A	63745	ICF0010-09C	1

SCALE

SHEET 1 OF 8

PRODUCT CONTROL DRAWING
66.7 AMP REMOTE POWER CONTROLLER
PRELIMINARY DATA

1.0 SCOPE:

This document describes a 66.7 A, 150 VDC remote power controller brass board for Martin Marietta. This brass board is constructed on a Eurocard format.

2.0 ELECTRICAL CHARACTERISTICS: (At 25°C unless otherwise specified)

2.1	Input	
2.1.1	Bias Supply Range	4.5 VDC min 5.5 VDC max
2.1.2	Bias Supply Current at 5 VDC	55 mA max
2.1.3	Reverse Polarity	-0.5 VDC
2.1.4	Maximum Turn-Off Voltage (Control)	1.1 V
2.1.5	Minimum Turn-On Voltage (Control)	1.7 V
2.1.6	Control Voltage Range	TTL Logic
2.1.7	Bit/Trip	TTL Logic
2.1.8	Status	TTL Logic
2.2	Output	
2.2.1	Load Current Rating (Forced Air)	66.7 A max
2.2.2	Continuous Blocking Voltage	180 VDC
2.2.3	Continuous Operating Output Voltage	150 VDC
2.2.4	Leakage Current at 150 VDC	2 mA max
2.2.5	Maximum On Resistance at 66.7 A	0.019 ohms max
2.2.6	Output Voltage Drop	1.27 V max
2.2.7	Turn-On Time	
2.2.7.1	Rise Time	300 usec typ
2.2.7.2	Time Delay On	100 usec typ
2.2.8	Turn-Off Time	
2.2.8.1	Fall Time	0.5 msec typ

SIZE	FSCM NO.	DWG. NO.	REV.
A	63745	ICF0010-09C	1
SCALE		SHEET 2	

2.2.8.2 Time Delay Off — 1.6 msec typ

2.2.9 Maximum Power Dissipation — 85 W

2.3 Short Circuit Protection

2.3.1 The RPC will not be damaged by a short on the load during normal operation or by being turned-on into a shorted load.

2.3.2 The RPC will not be damaged by a continuous overload condition (See Graph).

2.3.3 The RPC will automatically trip for current that exceeds 110% for more than 5 seconds (see Figure 1).

2.3.4 To return the RPC to a normal operating condition, remove the short circuit or overload condition, then remove and reapply the input control voltage.

2.4 Input-to-Output Dielectric Strength — 500 VAC max

REMOTE POWER CONTROLLER
OUTPUT CURRENT VS TIME TO TRIP

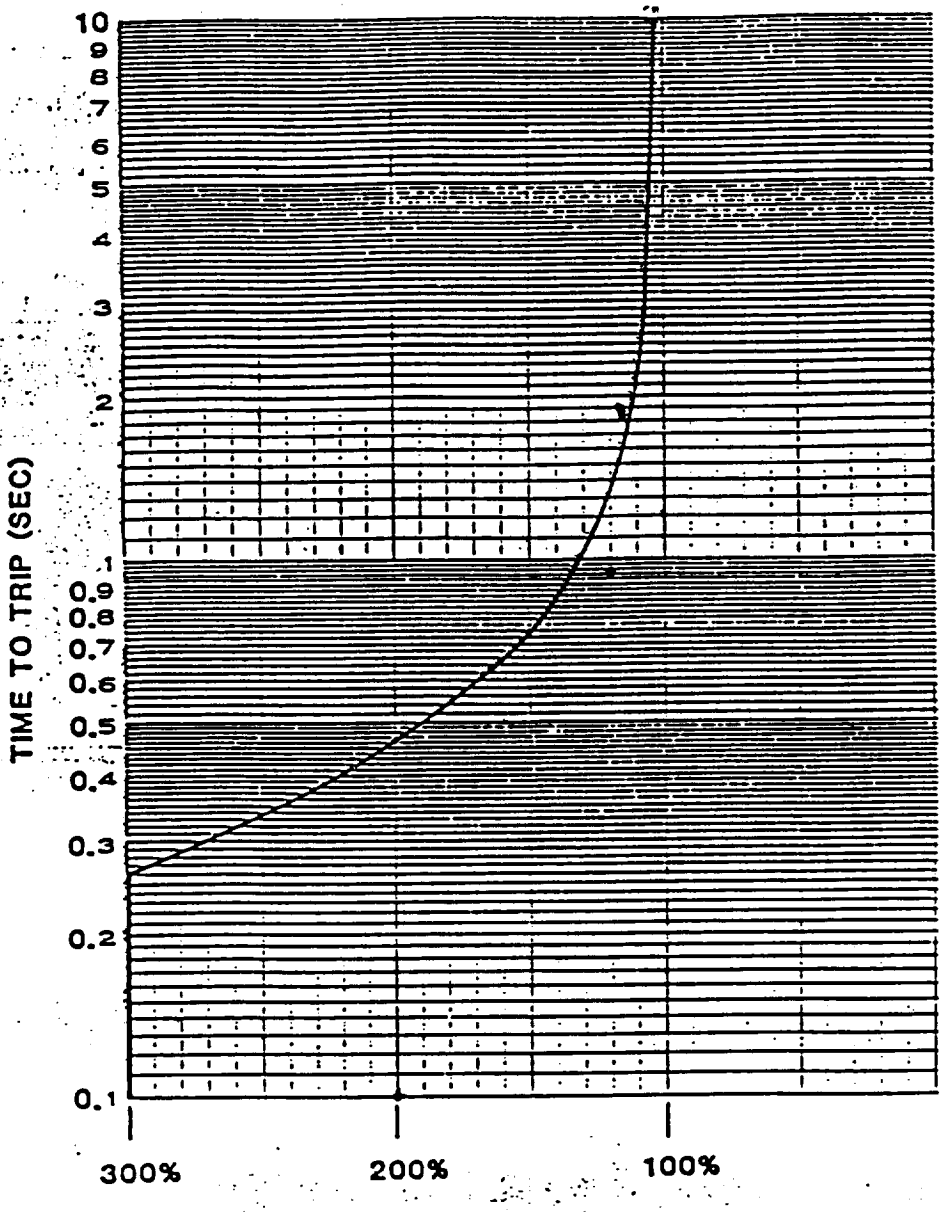


FIGURE 1

SIZE	FSCM NO.	DWG NO.	REV.
A	63745	ICF0010-09C	1
SCALE		SHEET 5	

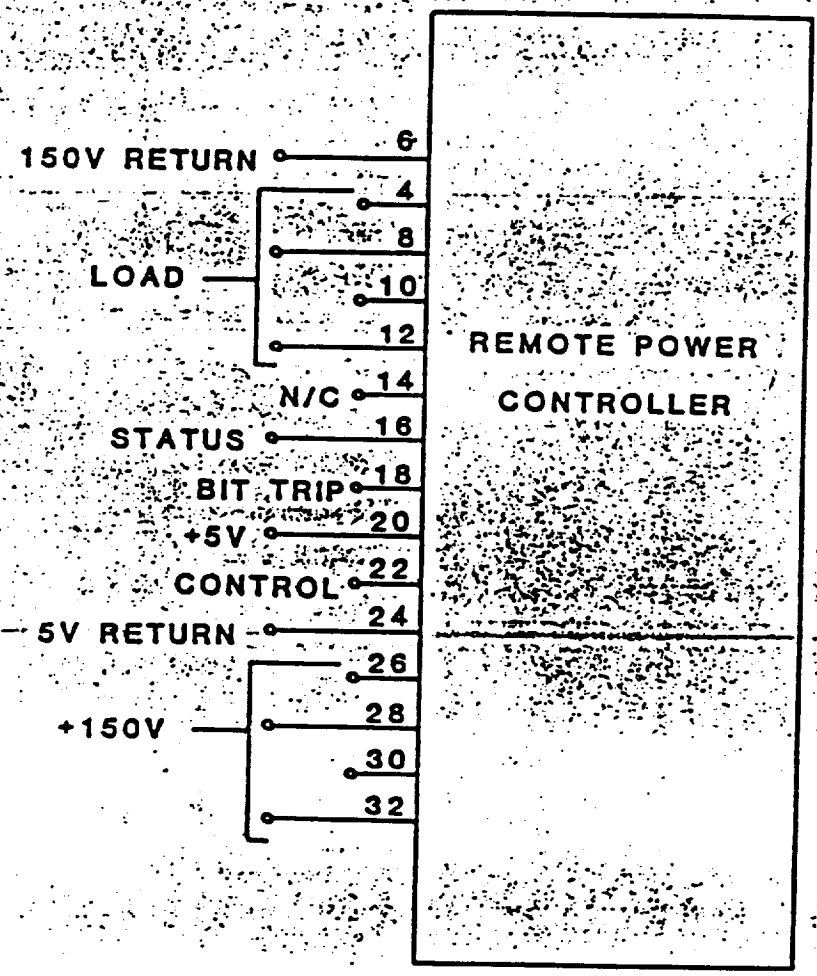
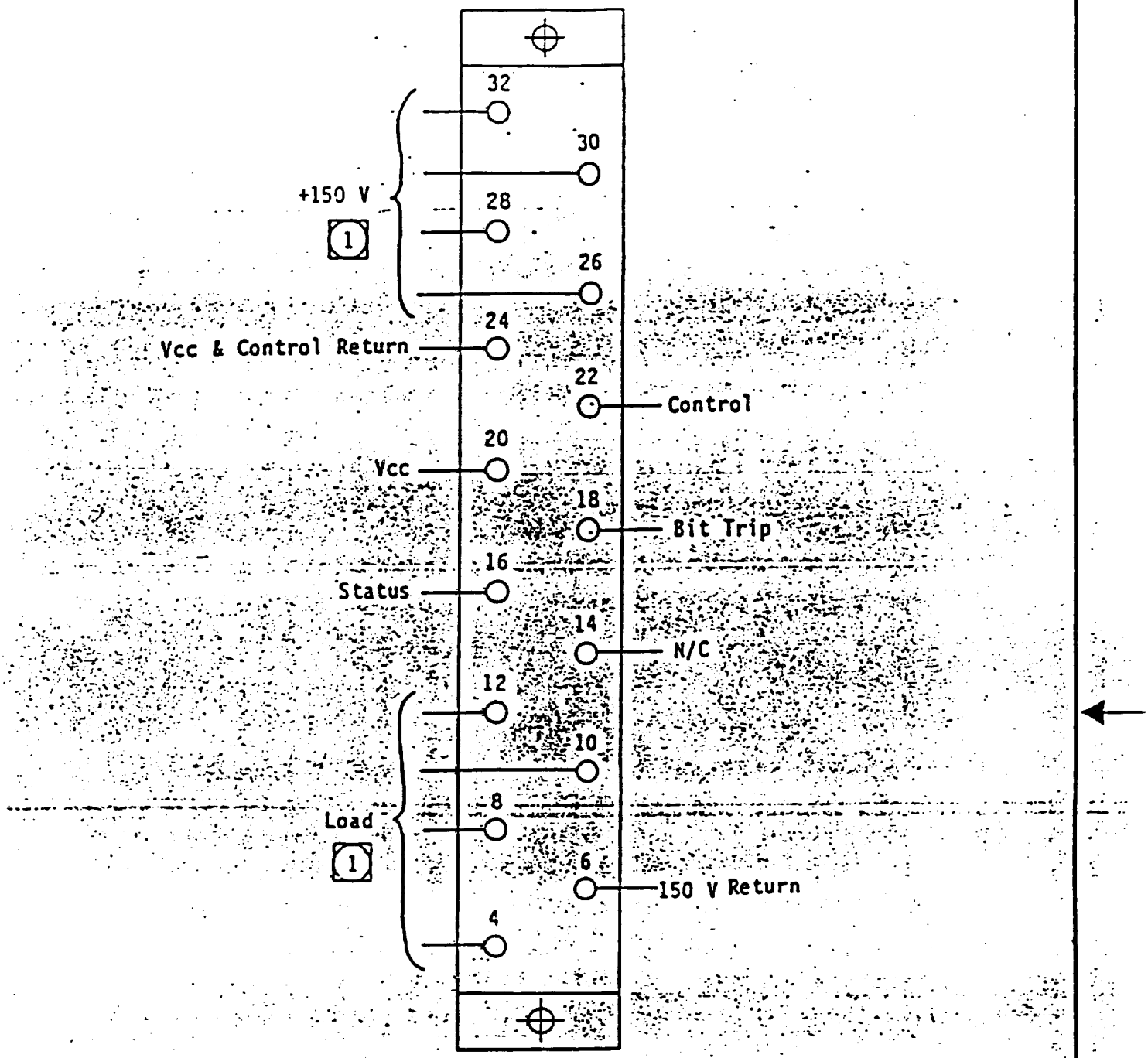


FIGURE 2

SIZE	FSCM NO.	DWG NO.	REV.
A	63745	ICF0010-09C	1
SCALE		SHEET 6	



1 To conduct rated current, all four of the indicated terminals are required.

FIGURE 3

SIZE	FSCM NO.	DWG NO.	REV.
A	63745	ICF0010-09C	1
SCALE		SHEET 7	

ORIGINAL PAGE IS OF POOR QUALITY

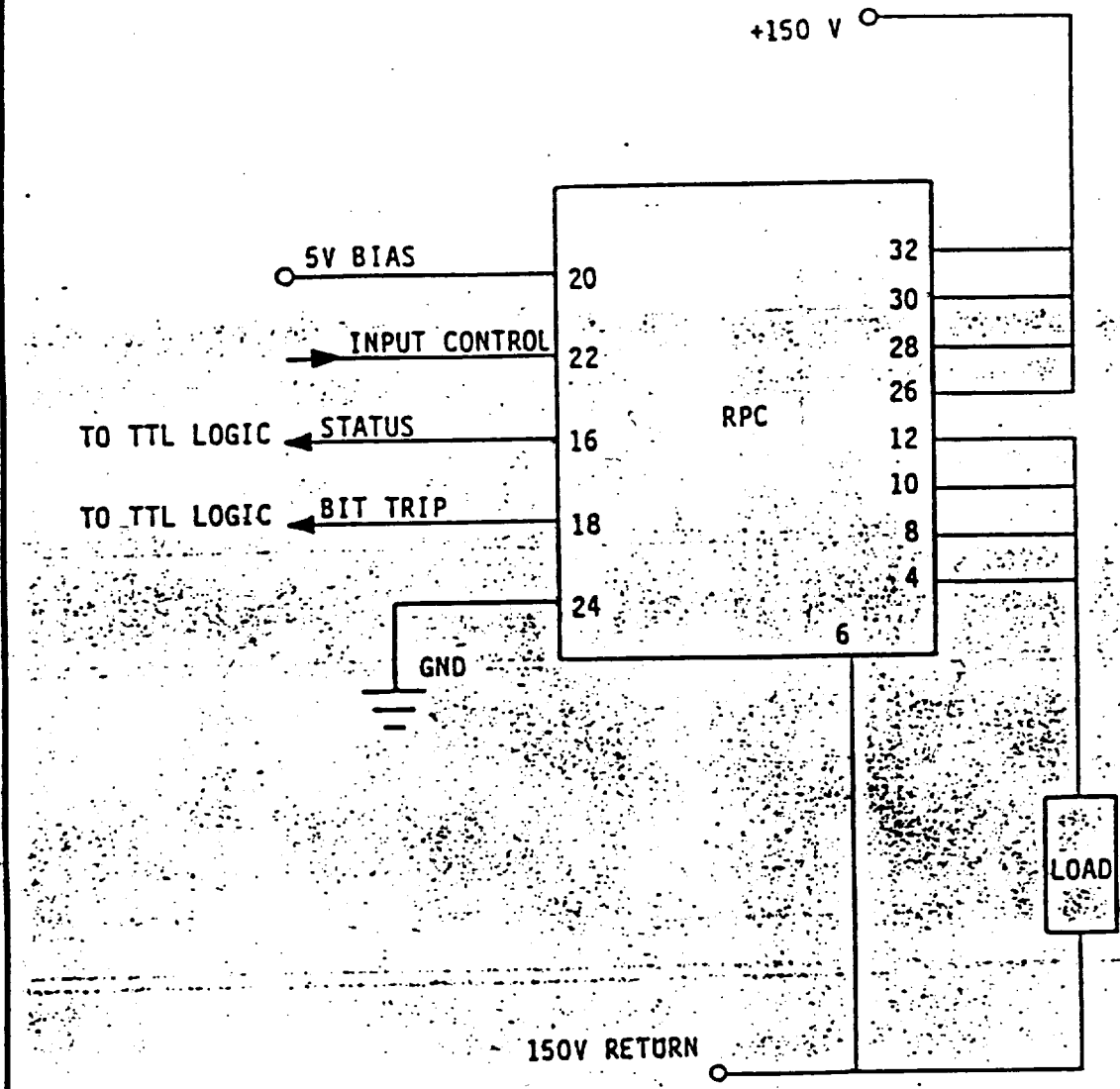


FIGURE 4

TYPICAL WIRING DIAGRAM

NOTE: To conduct rated current, four terminals at output must be tied together.

SIZE	FSCM NO.	DWG NO.	REV.
A	63745	ICF0010-09C	1
SCALE		SHEET 8 OF 8	

APPENDIX V

DC-400 Hz Load Converter Report

This report was produced as part of the previously deleted task of designing and breadboarding a DC-400 Hz load converter power supply.

NETWORK TOPOLOGY

LOAD CONVERTER

BREADBOARD

TEST REPORT

PREPARED BY

D.J. EASON

TABLE OF CONTENTS

EQUIPMENT LIST

EQUIPMENT TYPE	I.D. NUMBER	CAL. DUE DATE
Power supply 6227B Hewlett Packard	541812	Ref. only
Power supply LR 602 Lambda	529233	Ref. only
Power supply LPD 421 Lambda	542232	Ref. only
Function generator 3325A Hewlett Packard	551204	1-21-90
Oscilloscope 2465 Tektronix	550365	9-23-90
Oscilloscope 2430A Tektronix	556079	2-18-90
Current probe A6302 Tektronix	547332	2-25-90
Current probe A6302 Tektronix	152730	3-18-90
Probe amplifier AM503 Tektronix	550731	2-18-90
Probe amplifier AM503 Tektronix	536395	5-6-90
Power module TM501 Tektronix	547330	Ref. only
Power module TM501 Tektronix	540396	Ref. only
Freq. response analyzer Venable Ind. 5060	555474	Ref. only
Digital multimeter 193 Kiethley	552442	10-8-89

EQUIPMENT LIST (cont.)

EQUIPMENT TYPE	I.D. NUMBER	CAL. DUE DATE
Network analyzer 3577a Hewlett Packard	561848	Ref. only
Digital multimeter 87	153474	12-10-89

SCOPE

This report is intended to describe and assess the Network Topology Program Load Converter Breadboard test effort as it applies to proving the concept of the topology selected for the Load Converter. Also test data is presented with the intent of verifying compliance with Load Converter Design Goals (Ref. TEO-89-0251) on a down-scaled basis. Additional test data are given which do not neccessarily relate to specific design goals but are of interest with respect to power converters in general. Following the test data presentation a summary/conclusion is given and finally recommendations for improvement of the design are given. An appendix is included which provides engineering drawings, parts list, and data sheets.

FUCTIONAL DESCRIPTION

The Load Converter breadboard produces regulated sinusoidal AC output power from unregulated DC input power. The circuit consists of five functional blocks: pulse width modulator, drive stage, power stage, output stage, and feedback.

The pulse width modulator consists of an SG1524 PWM control chip. This chip contains a +5V reference, sawtooth oscillator, pulse width modulator with pulse metering and steering logic, and two complimentary open collector output drivers. A current limit circuit is also contained in the chip which is not used on the breadboard. Implementation of this function would be relatively fundamental and also desireable.

An external sinusoidal 400 Hz reference is fed into the error amplifier through a differential amplifier buffer. This signal and the power output voltage waveform are integrated through the error amplifier and the resultant signal is fed directly to the PWM. In the PWM chip the error signal is compared to the internally generated sawtooth oscillator signal. The result of this comparison is a pulse width modulated 400Hz sine wave. This signal is fed within the PWM chip to the output drivers.

The output drivers of the PWM chip are wire OR'ed to allow a duty cycle range of 0 to 100 per cent. A 74LS04 Hex Inverter chip is then utilized to produce complimentary full range (0 to 100%) signals. These complimentary signals are then fed to the gate drive stage of the circuit.

The gate drive stage of the breadboard consists of a DS0056 dual CMOS clock driver chip. This chip is designed to distribute high frequency clock signals to a large number of CMOS devices and is therefore ideal for driving a capacitive load such as a power MOSFET gate. The output of the driver chip is connected to the gate of the MOSFET through a 10 ohm resistor. The resistor limits current to and from the MOSFET gate and damps resonant LC circuit effects. The DS0056 driver greatly simplifies the gate drive design and helps keep the parts count low.

The power stage is composed of two power MOSFETs switching in complimentary fashion, and a power transformer with center tapped primary. The MOSFETs and power transformer are connected in a two-switch forward configuration as opposed to push-pull. Snubbers are utilized across each MOSFETs drain and source to minimize voltage spikes on the MOSFET drain with respect to ground. Pulse metering logic within the PWM chip assures a certain dead time is present between the two complimentary switching waveforms. This prevents both MOSFETs from turning on simultaneously which would effectively short the input power line to ground.

FUNCTIONAL DESCRIPTION (cont.)

The output consists of an LC low pass filter which has a corner frequency of 5kHz. This filter effectively attenuates switching frequency (77kHz) noise only. Since the synthesized (pulse width modulated) sine wave output of the power stage very closely resembles (harmonically) the precision sine wave reference there are no odd harmonics of the 400Hz fundamental,as in a square wave, to attenuate. This means the output filter components may be kept relatively small.

For feedback the output is sensed directly through a single operational amplifier differential amplifier which commutates an attenuated output voltage from the secondary or output to the primary or input side. The breadboard design allows approximatley 2.5k ohms of isolation between input and output. Relatively low values of resistance were used due to inavailability of high precision high resistance parts. The output of this circuit is fed to the error amplifier where the cycle described here begins again.

The houskeeping power for the breadboard and the sine wave reference were implemented with bench test equipment. Design of these circuits is not viewed as insurmountable.

RECOMMENDATIONS

Upon completion of Load Converter breadboard test a list of recommendations has been compiled. The following is a digest of that information. Along with each recommendation is given the reason or rationale for the recommended change.

The addition of a DC servo loop to keep the power transformer balanced must be investigated. This idea formulated when it was noticed that distortion of the output voltage waveform increased when the frequency response analyzer was inserted in the control loop. Further investigation revealed a switching current imbalance between the two MOSFET switches. It was determined that a slight adjustment of the DC offset of the sine wave reference remedied the problem. The DC servo loop recommended would sense the transformer voltage and feed an error signal to the sine wave reference thus making the system more robust and immune to adverse effects of test equipment such as frequency response analyzers.

A UC1707 gate drive I.C. should be icncorporated to replace the present two chip gate drive comprised of the 74LS04 and DS0056. Although the DS0056 greatly simplifies the gate drive design the UC1707 goes one step further by providing inverting and non inverting inputs. This means the use of the 74LS04 to produce comlimentary waveforms is no longer neccessary.

The use of METGLAS core material will improve efficiency of the converter. This recommendation is based upon computer analysis done on the Load Converter transformer in which several materials such as Permalloy 80, Supermendur, and METGLAS were compared. The METGLAS material was found to be much more efficient than others due to its ability to support a high flux density level thus making the transformer less massive.

An input LC filter should be incorporated to reduce conducted emissions. This filter must be designed to attenuate conducted emissions at 400Hz. This means the filter may be fairly large for single phase output application. Three phase applications would not require as large a filter due to higher frequency.

A precision sawtooth wave generator would reduce distortion of the output waveform. Although the breadboard exhibited low output distortion under most operating conditions harmonic distortion did become noticable under low input voltage and maximum load conditions. This meant that the sinusoidal error signal was nearly the same amplitude as the sawtooth wave. Non linearities near the peaks and valleys of the sawtooth wave caused distortion of the output. A precision sawtooth wave without or with less non linearity would not contribute to the distortion of the output.

RECOMMENDATIONS (cont.)

A current limit function should be incorporated. as mentioned in the Functional Description the current limit function of the PWM chip is not used. This would be a relatively trivial function to incorporate and is seen as a must in order for the converter to possess the ability to start a motor. Current programming of the power stage is an attractive option when considering this function due to the inherant current limiting of this approach. Other benefit are to be had with the current program approach as well: simplified control loop design due to single pole filter response for example.

The direct sense feedback amplifier must be redesigned using higher value resistors. This would improve isolation between input and output affording higher common mode voltage rejection in the system.

APPLICABLE DOCUMENTS

Technical discussion from change order #16	Enclosure 2 to TEO-89-0251
Engineering Procedures Directive	EPD 849MWT
Operations Directive	203627-100-20

BREADBOARD GOALS

The goal of the Load Converter breadboard is to prove the concept of a two switch forward converter with a sine wave reference producing sinusoidal output power.

This is a key milestone in the development of such a converter since this had never been done at MMAG. Secondary goals consisted of verifying parts stress levels and circuit performance with the idea that this data would drive design nuances previously unrecognized. These refinements are difficult to to identify and quantify through even the most rigorous analysis. Proof of the concept of the converter is believed to be a success and design refinements are given in the Recommendations section of this report.

SUMMARY

The Load Converter breadboard successfully produces well regulated, low distortion AC output power from unregulated DC input power. In conjunction with the recommended design changes discussed here it would be a simple matter of scaling up the basic design to achieve the original power level (175W) intended for the Load Converter. An on board sine wave reference is most likely the most significant task remaining. This along with on board housekeeping power capability would yield a fully self contained unit.

TEST DATA SECTION

EFFICIENCY AND REGULATION

EFFICIENCY

Min. line (10V) max. load (1 ohm).....21.1%

Nom. line (15V) max load (1 ohm).....18.6%

Max. line (20V) max. load (1 ohm).....16.8%

Note: There are two main contributors to the low efficiency of the breadboard: 1) Low output power level by design. 2) Output filter voltage drop; in a DC output converter this paramemter is negligible however with a 400Hz output the inductive reactance of the filter drops the output voltage seen at the load. Further investigation is required in this area to optimize filter characteristics.

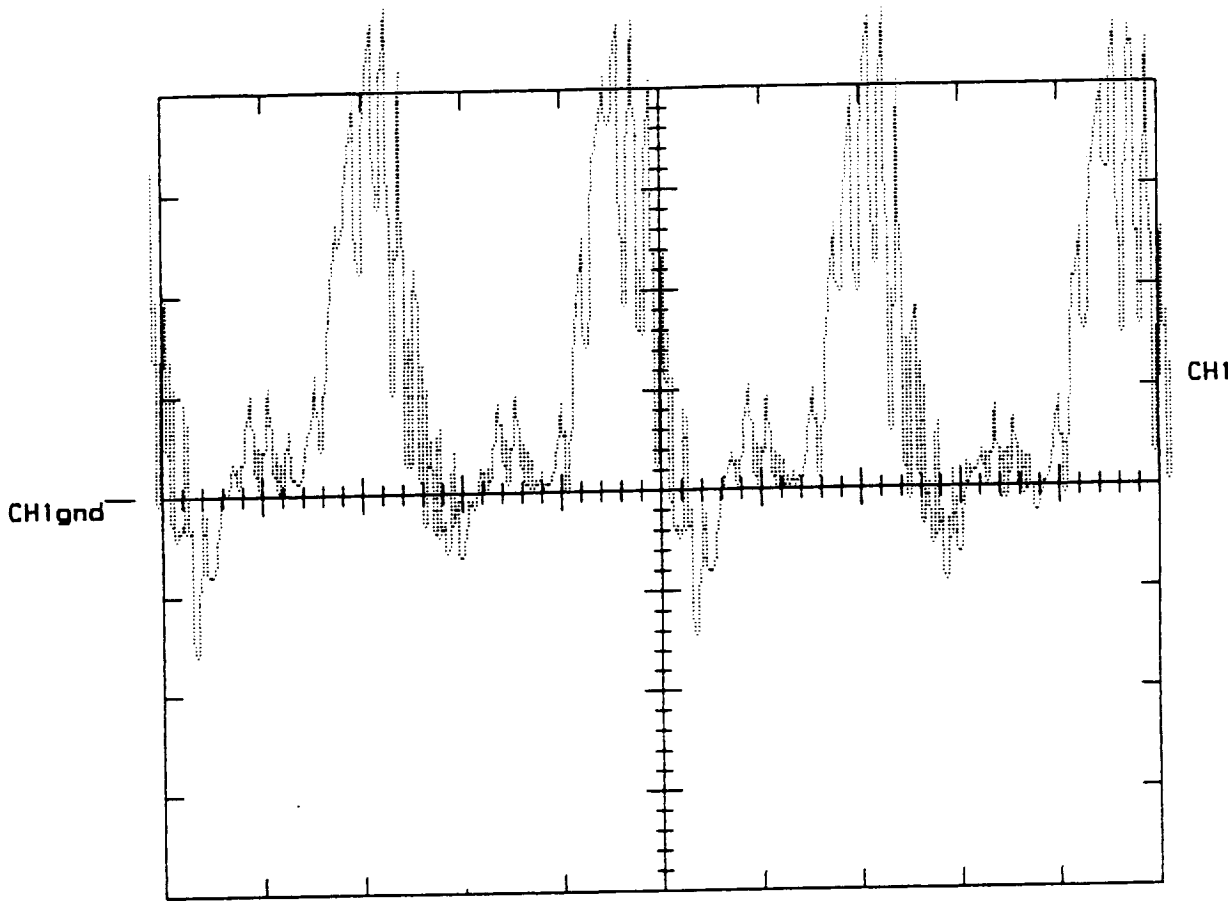
REGULATION

Min. line (10V) max. load (1 ohm).....Vout = 3.97 Vp-p

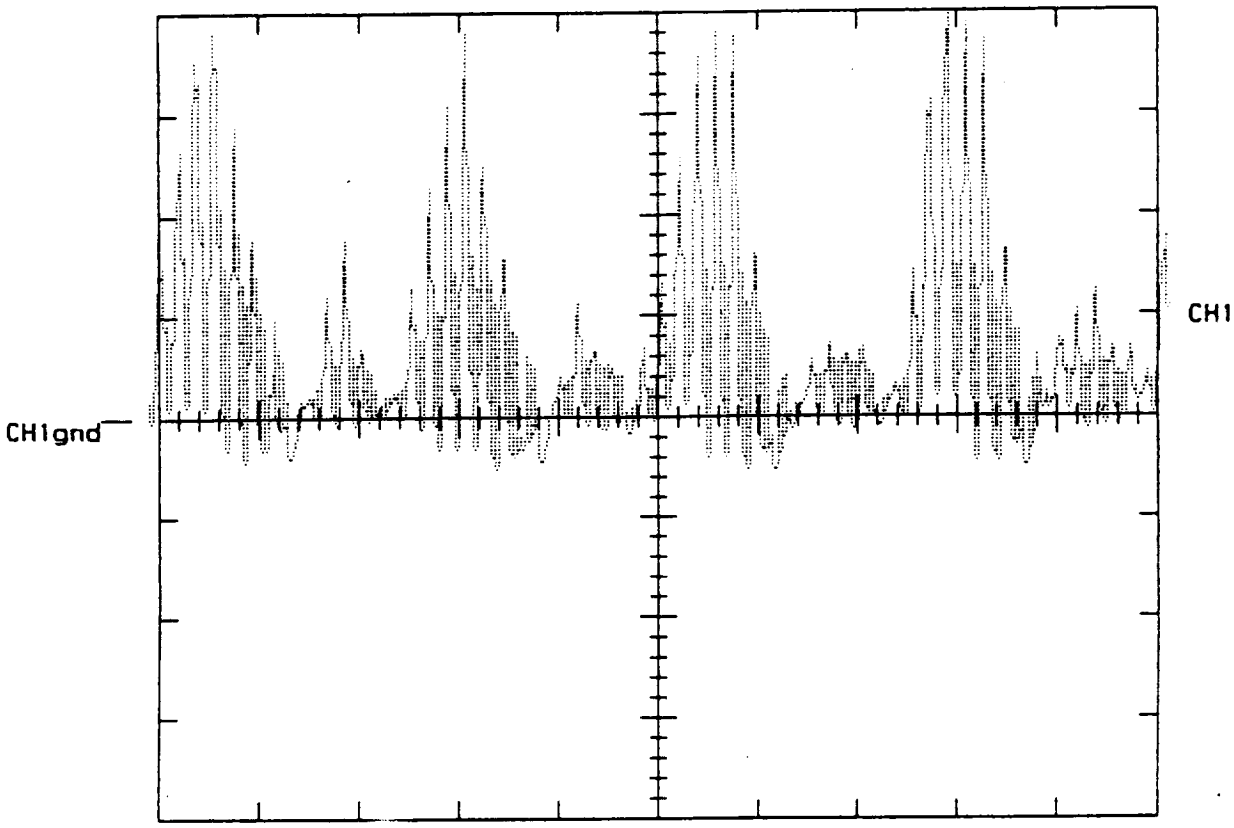
Max. line (20V) mav load (1 ohm).....Vout = 4.06 Vp-p

Line regulation.....2.2%

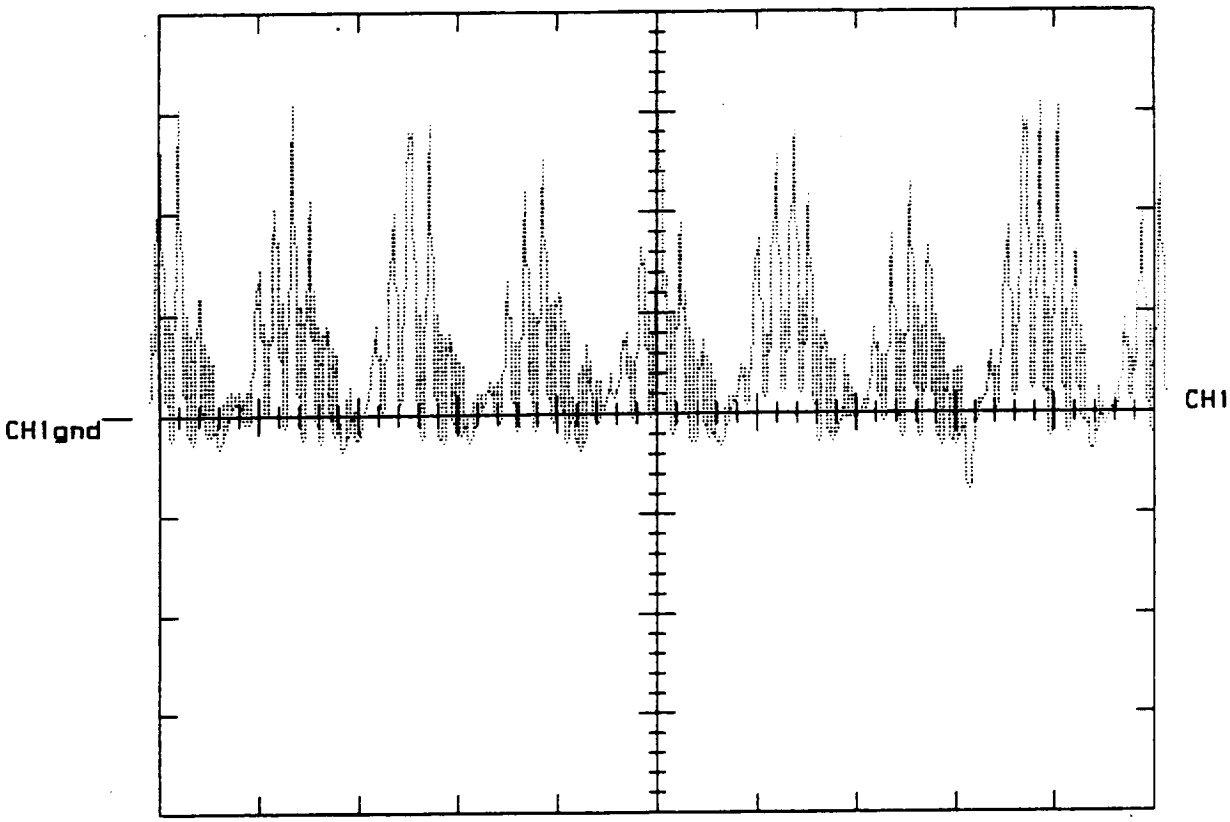
Load regulation from 10 ohms to 1 ohm (resistive) was less than one per cent including power factor excursion of 0.9 leading to 0.7 lagging.



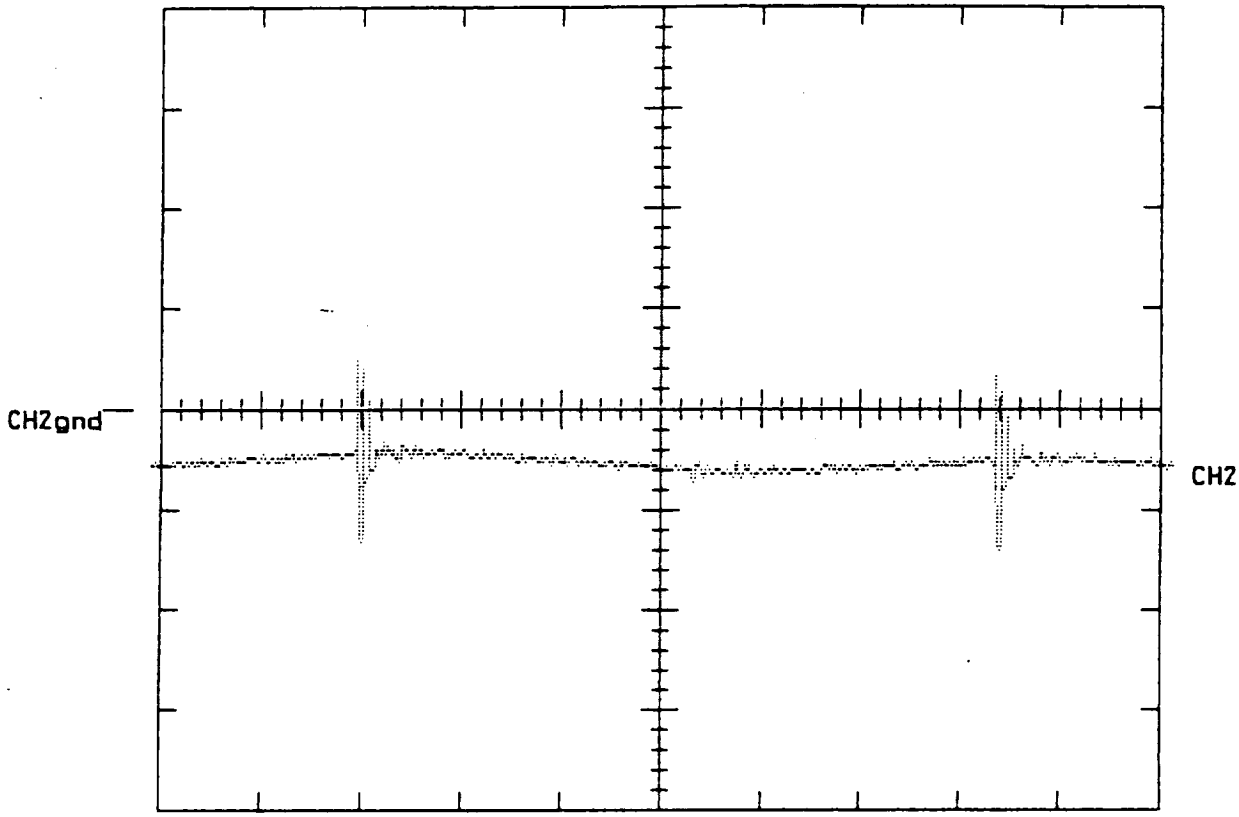
LINE CURRENT (CONDUCTED EMISSIONS)
Vin = 10 VDC (min. line)
max. load (1 ohm)
Verticle = 0.5A / div.
Horizontal = 1ms / div.



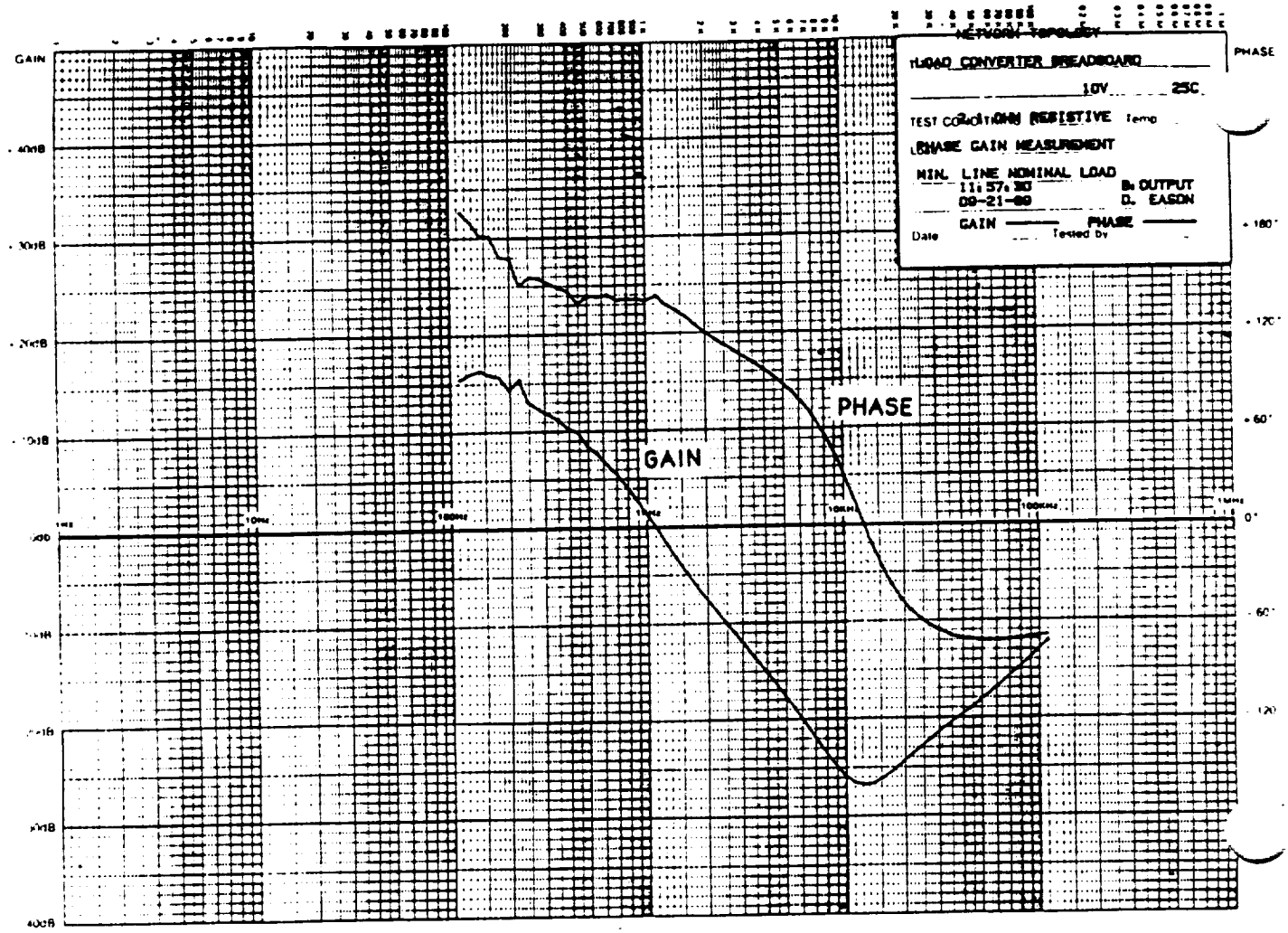
LINE CURRENT (CONDUCTED EMISSIONS)
Vin = 15 VDC (nom. line)
max. load (1 ohm)
Verticle = 0.5A / div.
Horizontal = 1ms / div.



LINE CURRENT (CONDUCTED EMISSIONS)
Vin = 20 VDC (max. line)
max. load (1 ohm)
Verticle = 0.5A / div.
Horizontal = 1ms / div.



OUTPUT VOLTAGE RIPPLE
Vin = 20 VDC (max. line)
MAXIMUM LOAD (1 ohm)
Verticle = 0.2V / div.
Horizontal = 2us / div.



OPEN LOOP PHASE GAIN MEASUREMENT
MIN. LINE (10V) MAX. LOAD (1 ohm)

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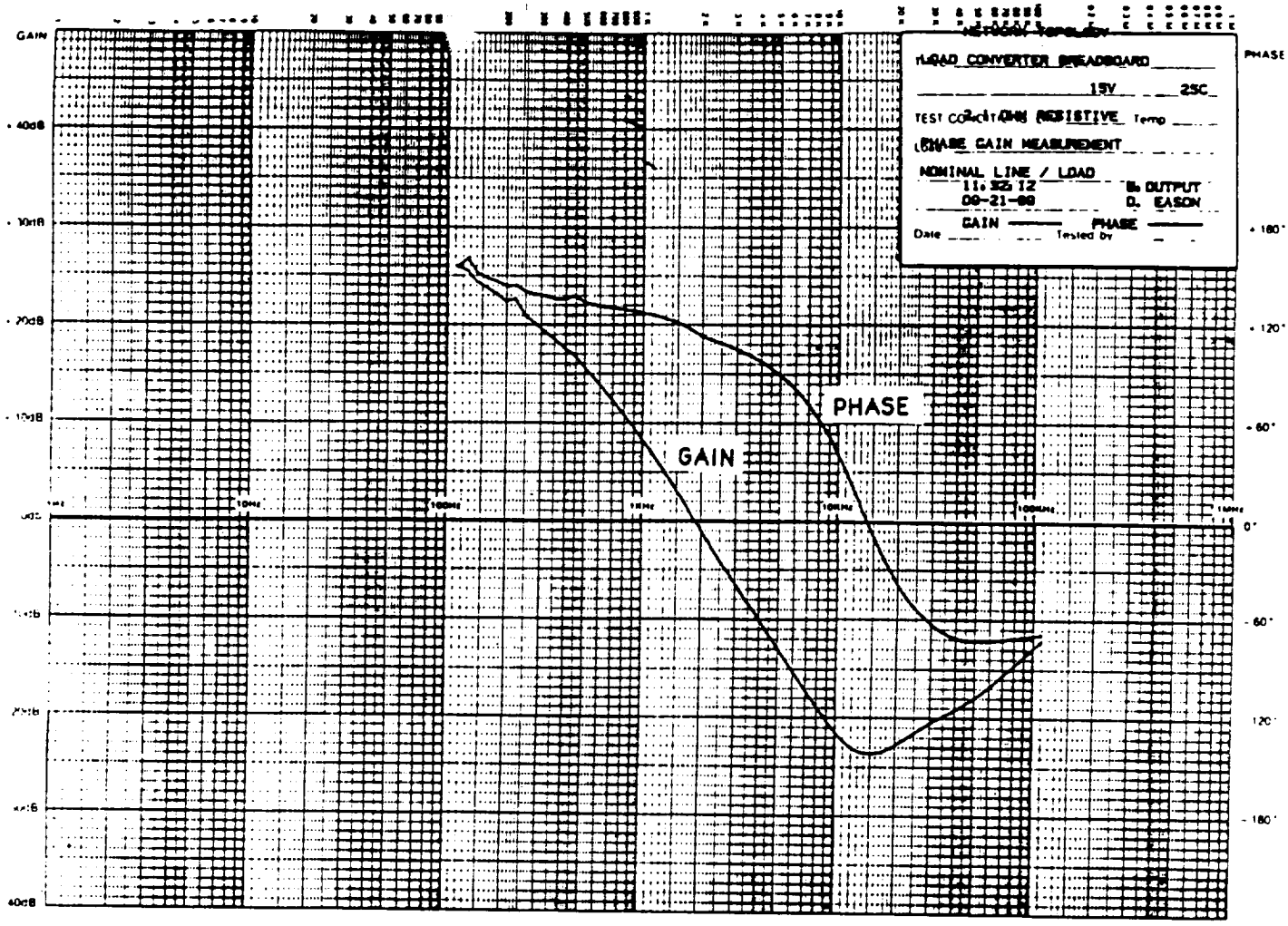

OPEN LOOP PHASE GAIN MEASUREMENT
NOM. LINE (15V) MAX. LOAD (1 ohm)

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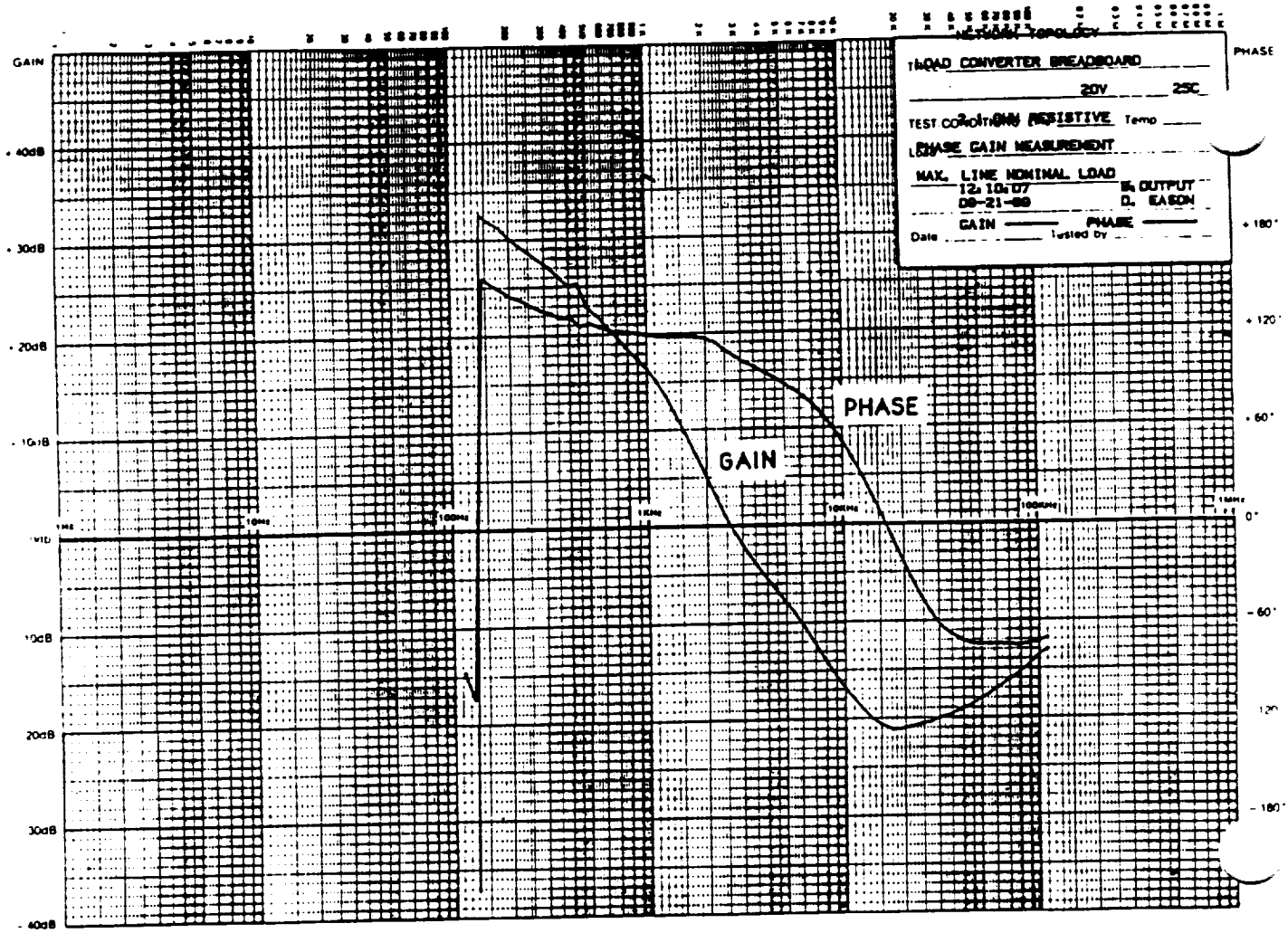
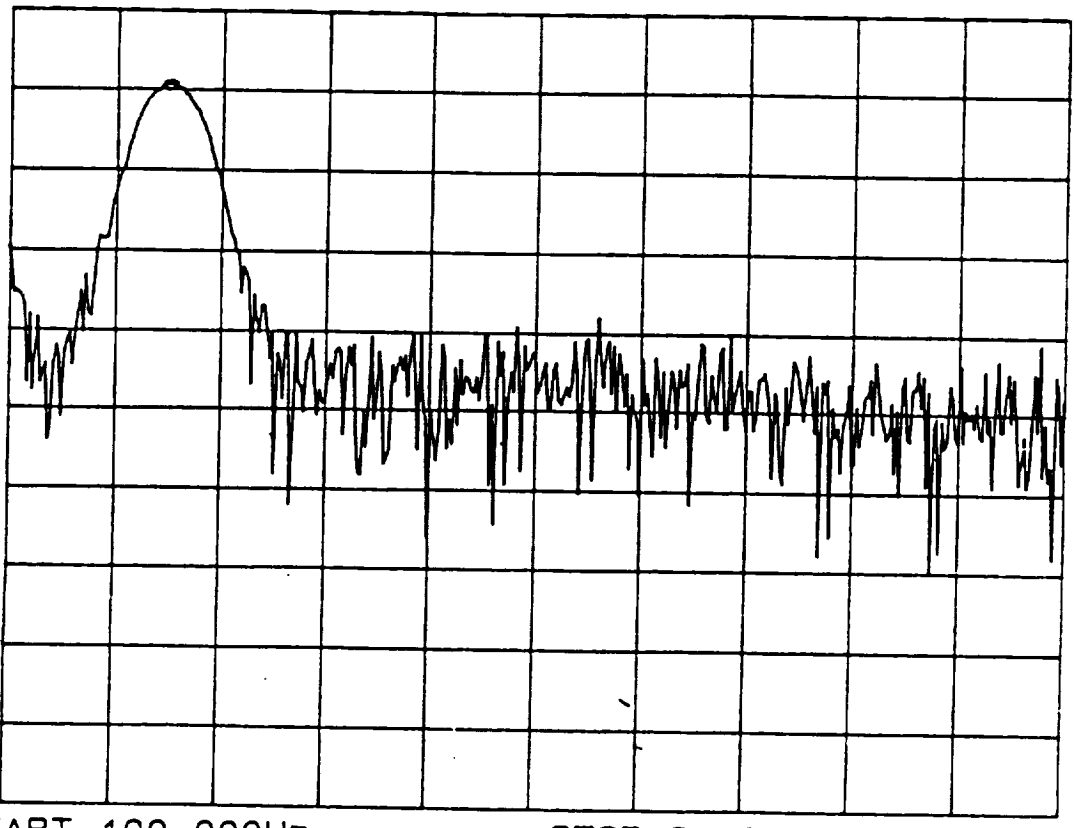


OPEN LOOP PHASE GAIN MEASUREMENT
MAX. LINE (20V) MAX. LOAD (1 ohm)

REF LEVEL
-60.000dBm

/DIV
10.000dB

MARKER 400.000Hz
MAG (R) -69.322dBm



START 100.000Hz
AMPTD -10.0dBm

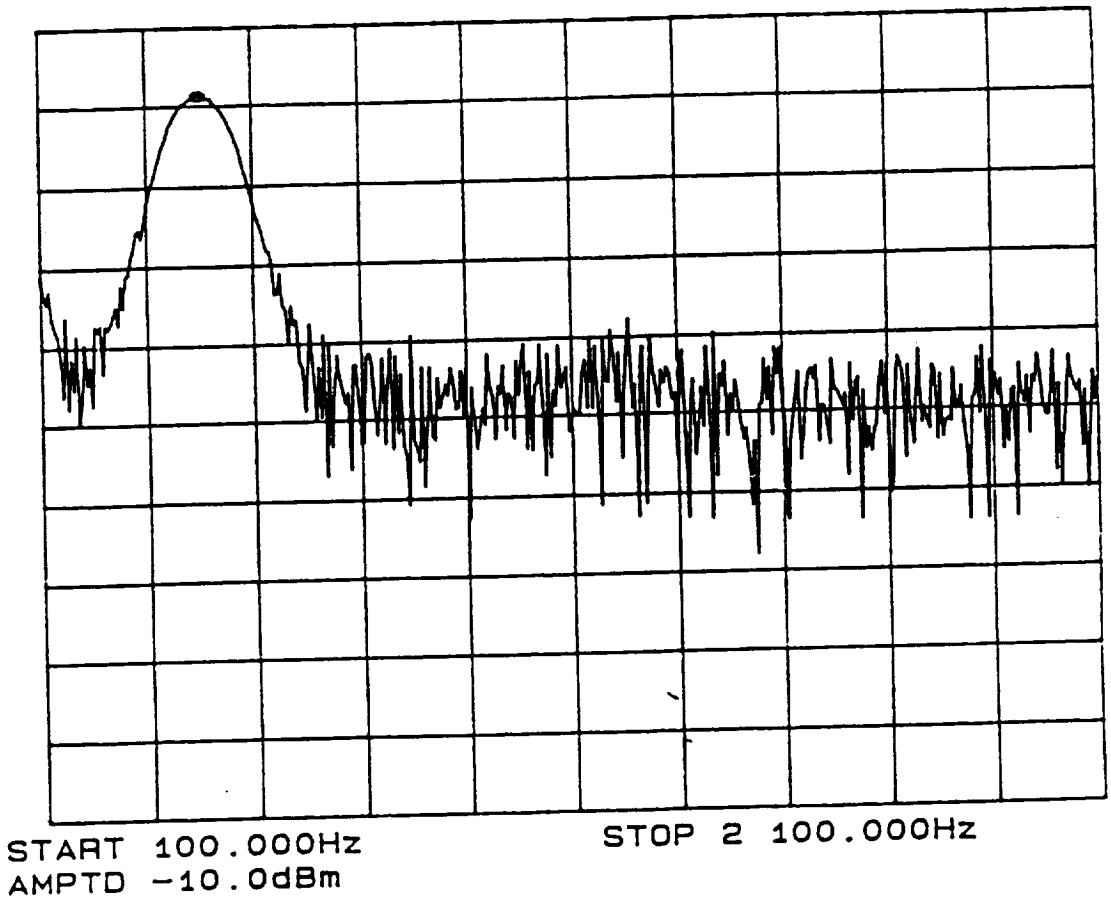
STOP 2 100.000Hz

OUTPUT VOLTAGE FREQUENCY SPECTRUM
MIN. LINE (10V) MAX LOAD (1 ohm)

REF LEVEL
-60.000dBm

/DIV
10.000dB

MARKER 400.000Hz
MAG (R)
-68.633dBm

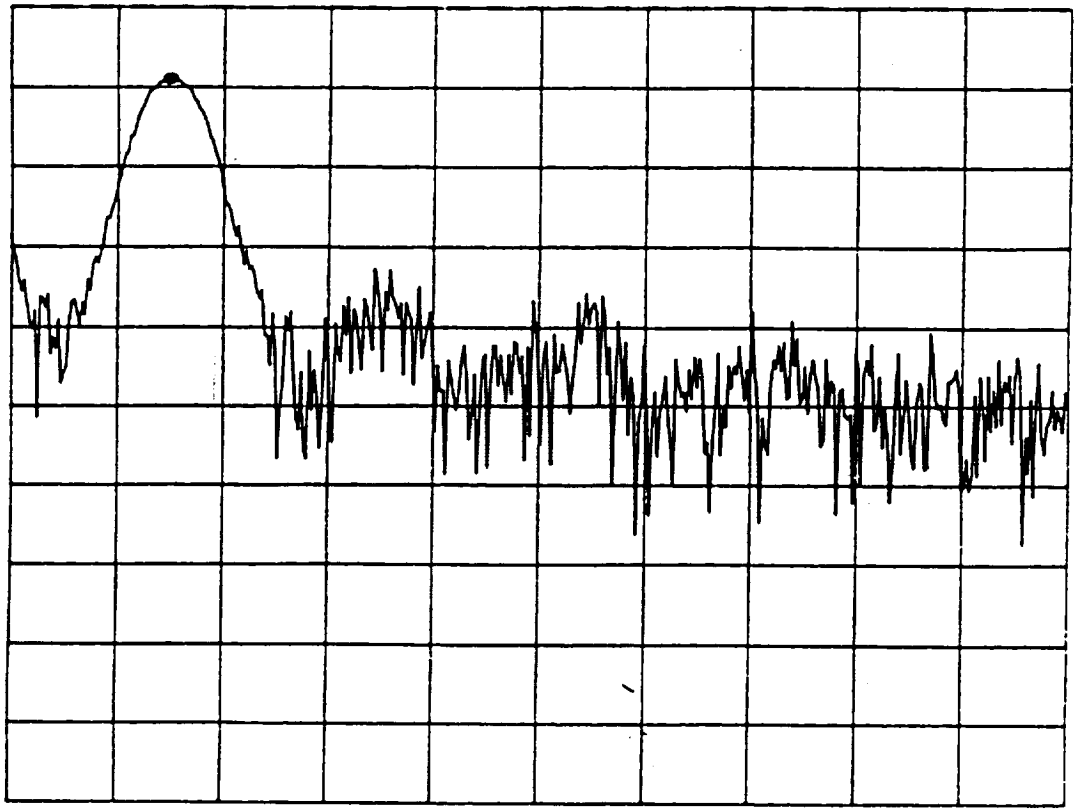


OUTPUT VOLTAGE FREQUENCY SPECTRUM
NOM. LINE (15V) MAX. LOAD (1 ohm)

REF LEVEL
-60.000dBm

/DIV
10.000dB

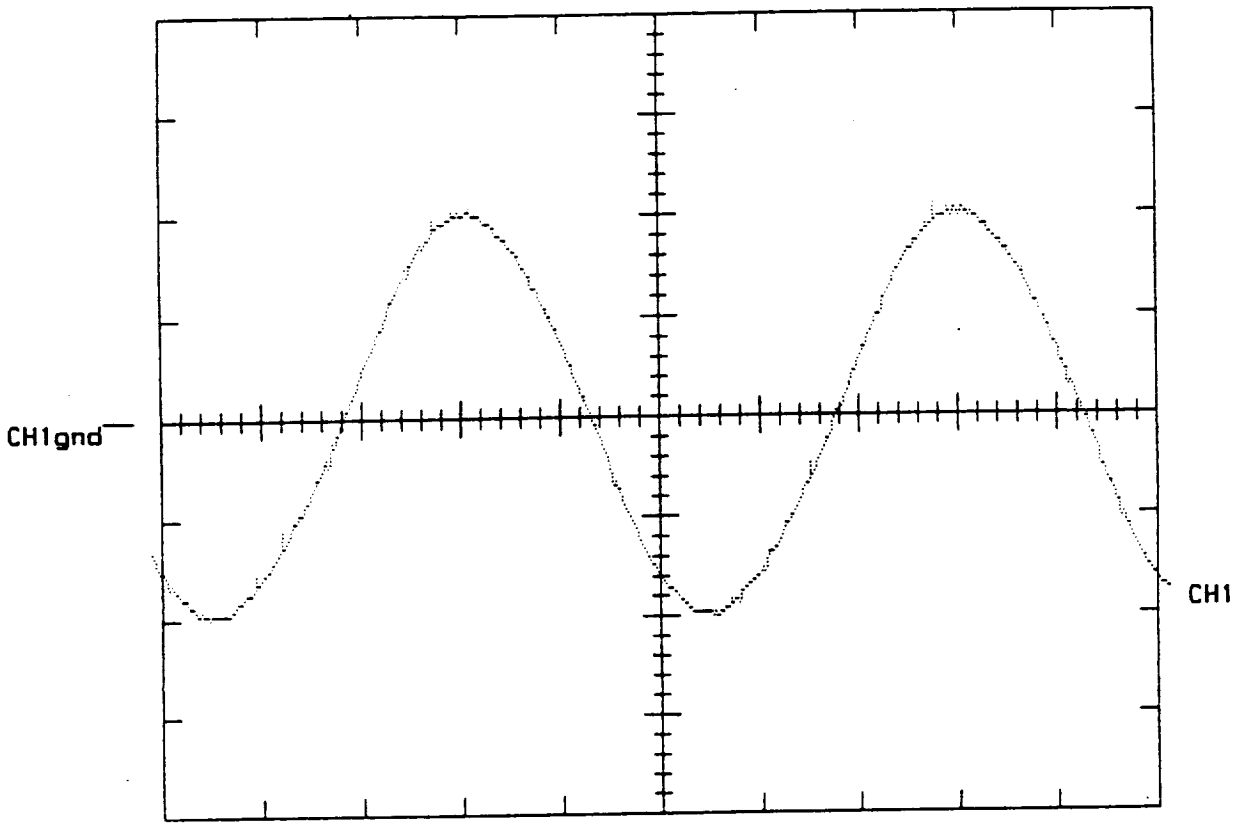
MARKER 400.000Hz
MAG (R)
-68.825dBm



START 100.000Hz
AMPTD -10.0dBm

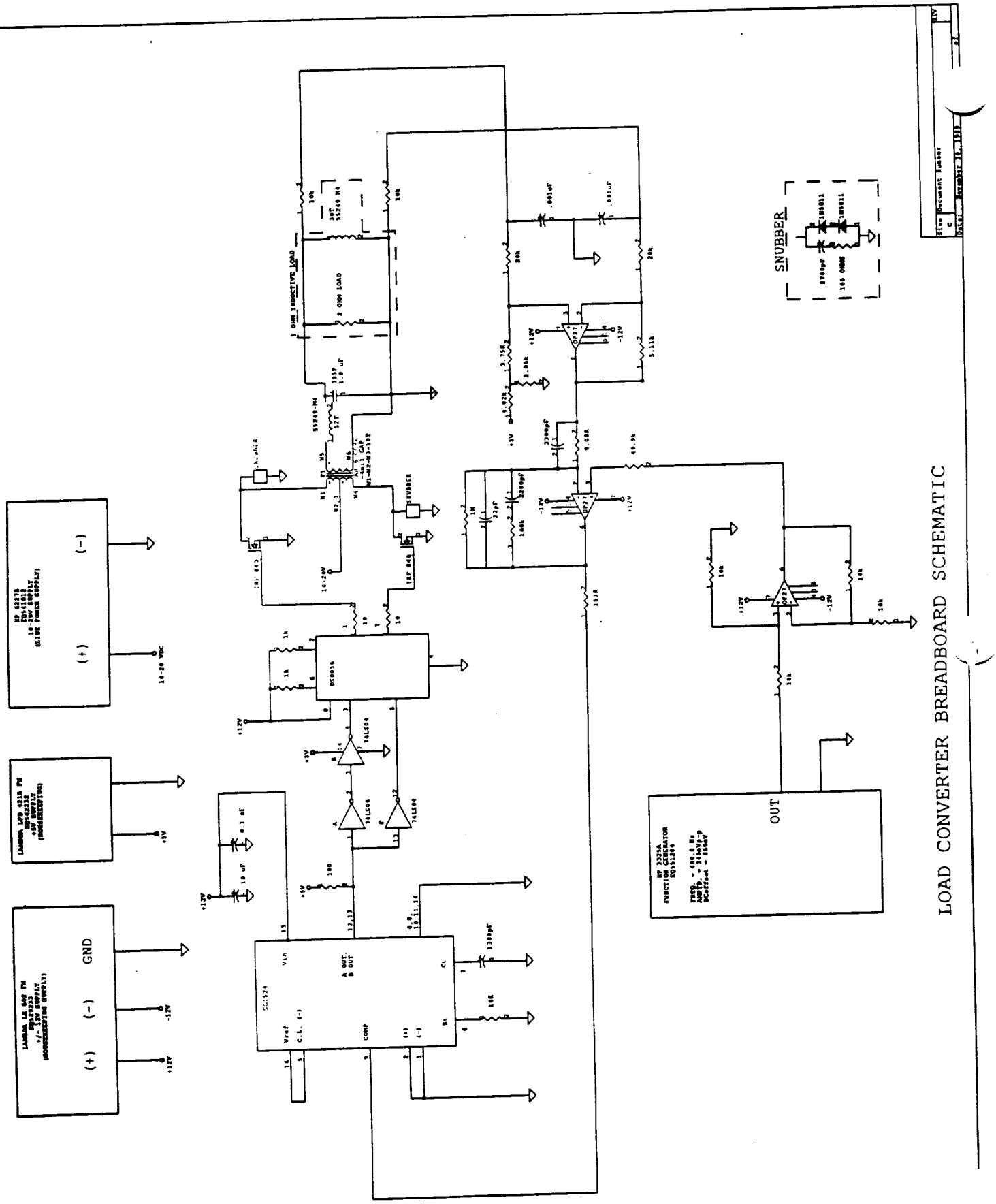
STOP 2 100.000Hz

OUTPUT VOLTAGE FREQUENCY SPECTRUM
MAX. LINE (20V) MAX. LOAD (1 ohm)



OUTPUT VOLTAGE
WAVEFORM
NOM. LINE (15V) MAX. LOAD (1 ohm)
Verticle = 1v/div.
Horizontal = 500us/div.

APPENDIX
ENGINEERING DRAWINGS
AND DATA SHEETS



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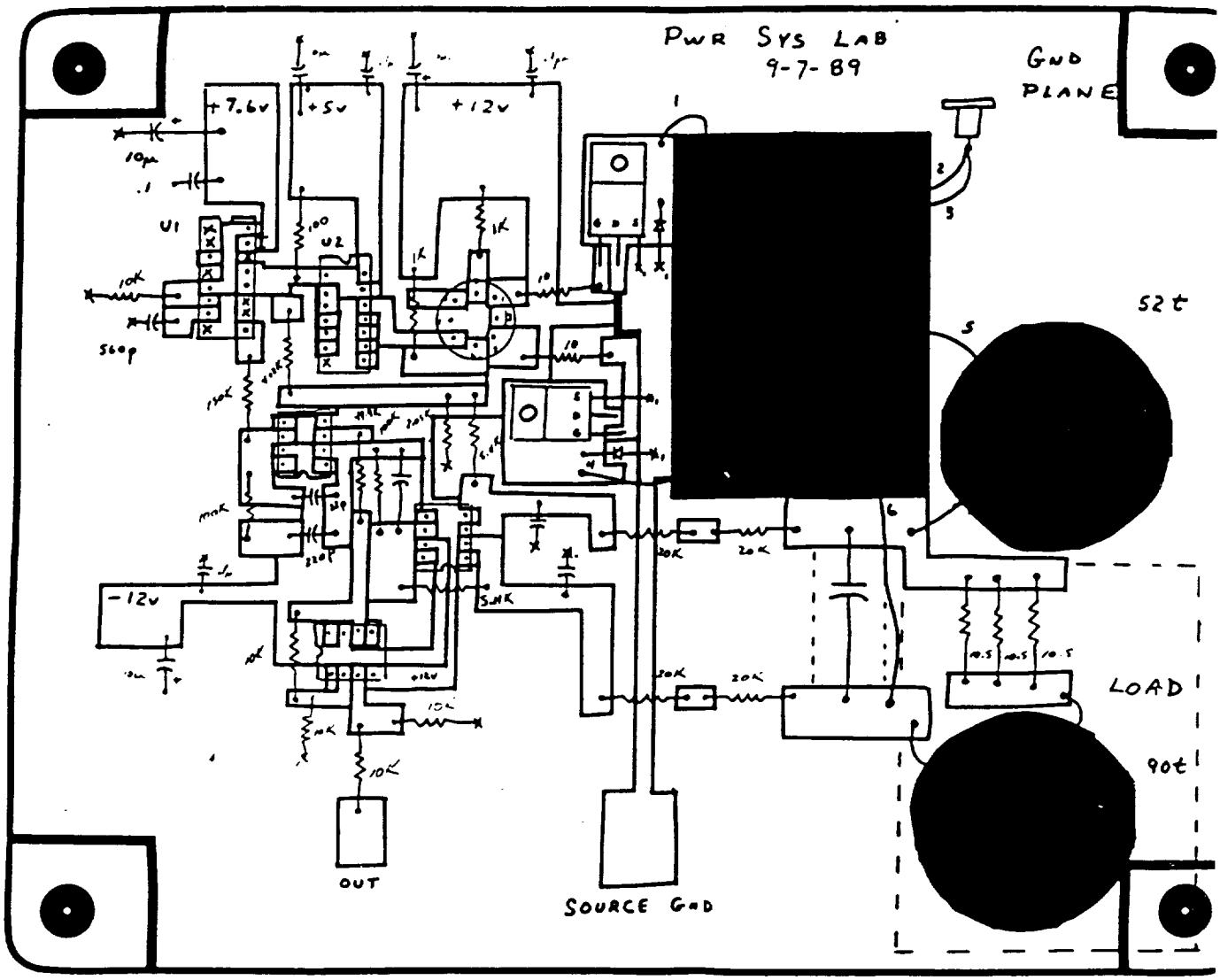
x = Gnd



Cp = 270 p

Load Converter
Breadboard
Layout Drawing

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1524/SG2524/SG3524

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power applications. The SG1524 is specified for operation over the full military ambient temperature range of -55°C to +125°C, the SG2524 for -25°C to +85°C, and the SG3524 is designed for commercial applications of 0°C to +70°C.

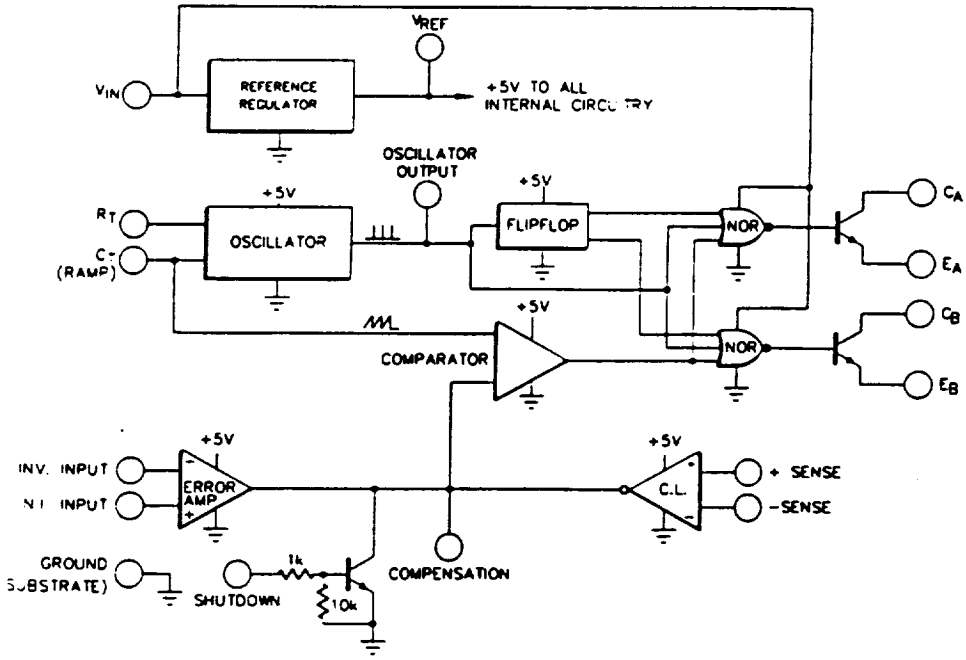
FEATURES

- 8V to 40V operation
- 5V reference
- Reference line and load regulation of 0.4%
- Reference temperature coefficient < ± 1%
- 100Hz to 300KHz oscillator range
- Excellent external sync capability
- Dual 50mA output transistors
- Current limit circuitry
- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Total supply current less than 10mA

HIGH RELIABILITY FEATURES - SG1524

- Available to MIL-STD-883B and DESC SMD
- MIL-M-38510/12601BEA - JAN1524J
- Radiation data available
- SG level "S" processing available

BLOCK DIAGRAM



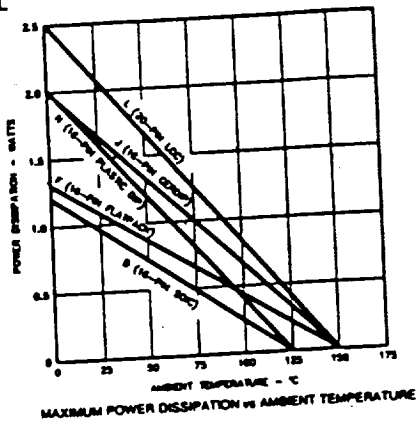
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage ($+V_{IN}$)	42V
Collector Voltage	40V
Logic Inputs	-0.3V to 5.5V
Current Limit Sense Inputs	-0.3V to 0.3V
Output Current (each transistor)	100mA
Reference Load Current	50mA
Oscillator Charging Current	5mA
Operating Junction Temperature	
Hermetic (J, F, L Packages)	175°C
Plastic (N, DW Packages)	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

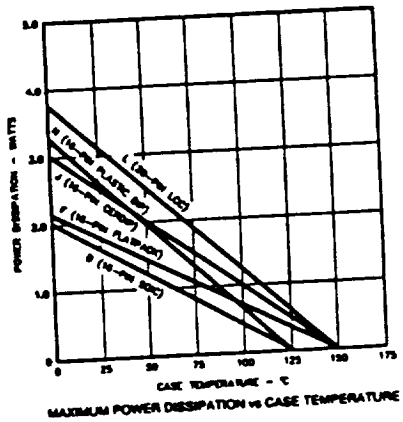
Note 1. Values beyond which damage may occur.

RECOMMENDED OPERATING CONDITIONS (Note 2)

THERMAL



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

ELECTRICAL

Input Voltage ($+V_{IN}$)	8V to 40V
Collector Voltage	0V to 40V
Error Amp Common Mode Range	1.8V to 3.4V
Current Limit Sense Common Mode Range	-0.3V to 0.3V
Output Current (each transistor)	0 to 50mA
Reference Load Current	0 to 20mA
Oscillator Charging Current	30μA to 2mA
Oscillator Frequency Range	100Hz to 300KHz
Oscillator Timing Resistor (R_T)	1.8KΩ to 100KΩ
Oscillator Timing Capacitor (C_T)	1nF to 1.0μF
Operating Ambient Temperature Range	
SG1524	-55°C to 125°C
SG2524	-25°C to 85°C
SG3524	0°C to 70°C

Note 2: Range over which the device is funcional and parameter limits are guaranteed.

ELECTRICAL SPECIFICATIONS

($+V_{IN}$ = 20V, and over operating temperature, unless otherwise specified.)

Parameter	Test Conditions	SG1524/2524 Min.	SG1524/2524 Typ.	SG1524/2524 Max.	SG3524 Min.	SG3524 Typ.	SG3524 Max.	Units
Reference Section (Note 3)								
Output Voltage	T_J = 25°C	4.80	5.00	5.20	4.60	5.00	5.40	V
Line Regulation	V_{IN} = 8V to 40V			20			30	mV
Load Regulation	I_L = 0 to 20mA			50			50	mV
Temperature Stability (Note 7)	Over Operating Temperature Range			50			50	mV
Total Output Voltage Range (Note 7)	Over Line, Load and Temperature	4.80		5.20	4.60		5.40	V
Short Circuit Current	V_{REF} = 0V	25	50	150	25	50	150	mA

Note 3. I_L = 0mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1524/2524 Min.	SG1524/2524 Typ.	SG1524/2524 Max.	SG3524 Min.	SG3524 Typ.	SG3524 Max.	Units
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	36	40	44	36	40	44	KHz
	MIN ≤ T_J ≤ MAX	34		46	34		46	KHz
Voltage Stability	V_{IN} = 8V to 40V		0.1	1		0.1	1	%
Maximum Frequency	R_T = 2KΩ, C_T = 1nF	200	400		200	400		KHz
Sawtooth Peak Voltage	V_{IN} = 40V	3		3.8	3		3.8	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.6	1	1.2	0.6	1	1.2	V
Clock Amplitude		3.2			3.2			V
Clock Pulse Width		0.3		1.5	0.3		1.5	µs
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2KΩ		0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			2	µA
DC Open Loop Gain	R_L ≥10MΩ, T_J = 25°C	72			60			dB
Output Low Level	V_{PIN1} - V_{PIN2} ≥ 150mV		0.2	0.5		0.2	0.5	V
Output High Level	V_{PIN2} - V_{PIN1} ≥150mV	3.8	4.2		3.8	4.2		V
Common Mode Rejection	V_{CM} = 1.8V to 3.4V	70						dB
Supply Voltage Rejection	V_{IN} = 8V to 40V	55						dB
Gain-Bandwidth Product (Note 7)	T_J = 25°C	1	2		1	2		MHz
P.W.M. Comparator (Note 4)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Current Limit Amplifier Section (Note 6)								
Sense Voltage	T_J = 25°C	190	200	210	180	200	220	mV
Input Bias Current				200			200	µA
Shutdown Section								
Threshold Voltage	T_J = 25°C	0.5	0.8	1.2	0.5	0.8	1.2	V
	MIN ≤ T_J ≤ MAX	0.2		1.8	0.2		1.8	V
Output Section (each transistor)								
Collector Leakage Current	V_{CE} = 40V			50			50	µA
Collector Saturation Voltage	I_C = 50mA			2			2	V
Emitter Output Voltage	I_E = 50mA	17			17			V
Collector Voltage Rise Time	R_C = 2KΩ			0.4			0.4	µs
Collector Voltage Fall Time	R_C = 2KΩ			0.2			0.2	µs
Power Consumption								
Standby Current	V_{IN} =40V		7	10		7	10	mA

Note 4. F_{OSC} = 40KHz (R_T = 2.9KΩ, C_T = .01µF)
Note 5. V_{CM} = 2.5V
Note 6. V_{CM} = 0V
Note 7. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

APPLICATION NOTES

OSCILLATOR

The oscillator in the SG1524 uses an external resistor R_T to establish a constant charging current into an external capacitor C_T. While this uses more current than a series-connected RC, it provides a linear ramp voltage at C_T which is used as a time-dependent reference for the PWM comparator. The charging current is equal to $3.6V/R_T$, and should be restricted to between 30µA and 2mA. The equivalent range for R_T is 1.8K to 100K.

The range of values for C_T also has limits, as the discharge time of C_T determines the pulse width of the oscillator output pulse. The pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output deadtime relationship is shown in Figure 1. A pulse width below 0.35 microseconds may cause failure of the internal flip-flop to toggle. This restricts the minimum value of C_T to 1000pF. (Note: Although the oscillator output is a convenient oscilloscope sync input, the probe capacitance will increase the pulse width and decrease the oscillator frequency slightly.) Obviously, the upper limit to the pulse width is determined by the modulation range required in the power supply at the chosen switching frequency. Practical values of C_T fall between 1000pF and 0.1µF, although successful 120 Hz oscillators have been implemented with values up to 5µF and a series surge limit resistor of 100 ohms.

The oscillator frequency is approximately $1/R_T \cdot C_T$; where R is in ohms, C is in microfarads, and the frequency is in Megahertz. For greater accuracy, the chart in Figure 2 may be used for a wide range of operating frequencies.

Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. For push-pull applications, the outputs are used separately; the flip-flop limits the duty cycle range at each output to 0-45%, and the effective switching frequency at the transformer is 1/2 the oscillator frequency.

If it is desired to synchronize the SG1524 to an external clock, a positive pulse may be applied to the clock pin. The oscillator should be programmed with R_T and C_T values that cause it to free-run at 90% of the external sync frequency. A sync pulse with a maximum logic 0 of +0.3 volts and a minimum logic 1 of +2.4 volts applied to Pin 3 will lock the oscillator to the external source. The minimum sync pulsewidth should be 200 nanoseconds, and the maximum is determined by the required deadtime. The clock pin should never be driven more negative than -0.3 volts, nor more positive than +5.0 volts. The nominal resistance to ground is 3.2K at the clock pin, ±25% over temperature.

If two or more SG1524s must be synchronized together, program one master unit with R_T and C_T for the desired frequency. Leave the R_T pins on the slaves open, connect the C_T pins to the C_T of the master, and connect the clock pins to the clock pin of the master. Since C_T is a high-impedance node, this sync technique works best when all devices are close together.

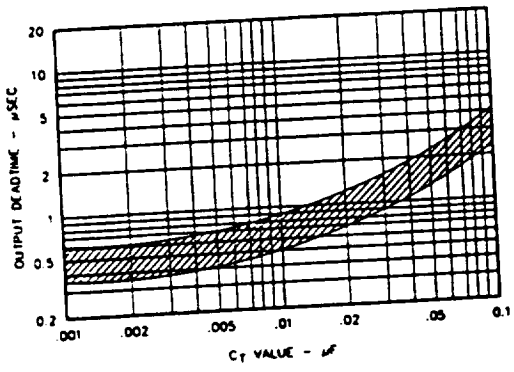


FIGURE 1 - OUTPUT STAGE DEADTIME VS. C_T

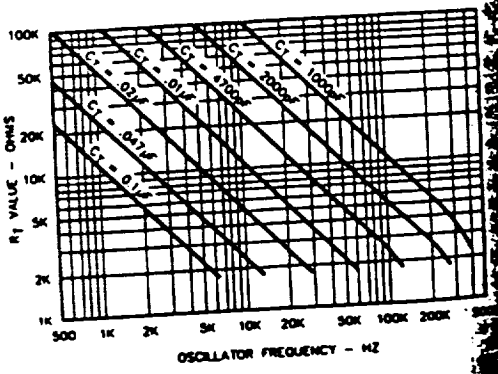


FIGURE 2 - OSCILLATOR FREQUENCY VS. R_T AND C_T

APPLICATION NOTES (continued)

CURRENT LIMITING

The current limiting circuitry of the SG1524 is shown in Figure 3. By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R1:

$$\text{C.L. Threshold} = V_{BE}(Q1) + I_1 \cdot R_2 - V_{BE}(Q2) = I_1 \cdot R_2$$
$$\sim 200\ \text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use because of its simplicity.

The most important of these is the limited common-mode voltage range: ±0.3 volts around ground. This requires sensing in the ground or return line of the power supply. Also precautions should be taken to not turn on the parasitic substrate diode of the integrated circuit, even under transient conditions. A Schottky clamp diode at Pin 5 may be required in some configurations to achieve this.

A second factor to consider is that the response time is relatively slow. The current limit amplifier is internally compensated by R_1, C_1, and Q1, resulting in a roll-off pole at approximately 300 Hz.

A third factor to consider is the bias current of the C.L. Sense pins. A constant current of approximately 150µA flows out of Pin 4, and a variable current with a range of 0-150µA flows out of Pin 5. As a result, the equivalent source impedance seen by the current sense pins should be less than 50 ohms to keep the threshold error less than 5%.

Since the gain of this circuit is relatively low (42 dB), there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle (+2 volts at the error amplifier output) with the error amplifier signaling maximum duty cycle.

APPLICATION NOTE: If the current limit function is not used on the SG1524, the common-mode voltage range restriction requires both current sense pins to be grounded.

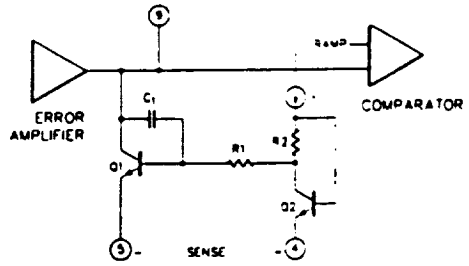
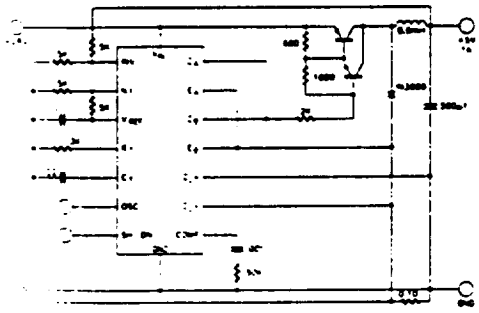
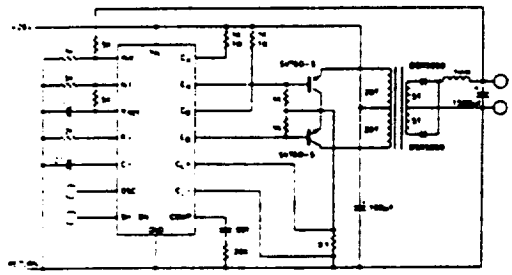


FIGURE 3 - CURRENT LIMITING CIRCUITRY OF THE SG1524

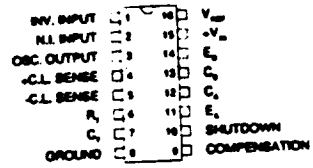
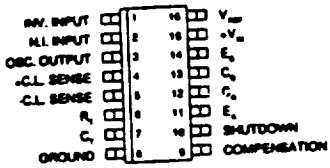
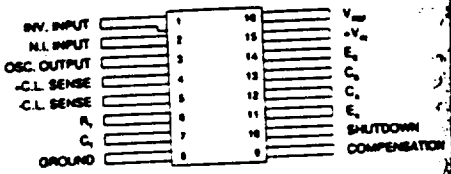
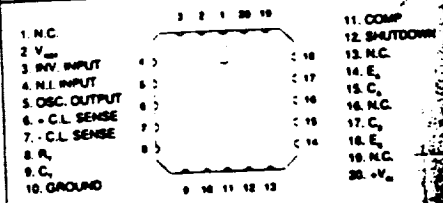


In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective 0 - 90% duty-cycle modulation. The use of an output inductor requires and R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1524J/883B SG1524J SG2524J SG3524J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2524N SG3524N	-25°C to 85°C 0°C to 70°C	
16-PIN NARROW BODY PLASTIC S.O.I.C. D - PACKAGE	SG2524D SG3524D	-25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG1524F/883B SG1524F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1524L/883B SG1524L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All packages are viewed from the top.

National Semiconductor

MOS Memory Interface Circuits

DS0026, DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76A.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to $(V^+ - 0.1V)$ in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

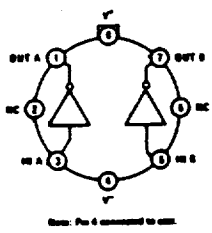
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

Features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

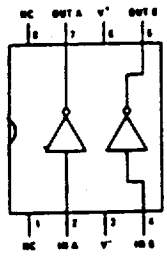
Connection Diagrams (Top Views)

TO-5 Package



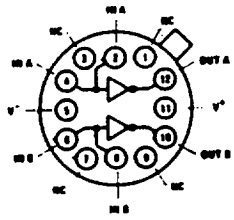
Order Number DS0026H
or DS0026CH
See NS Package H08C

Dual-In-Line Package



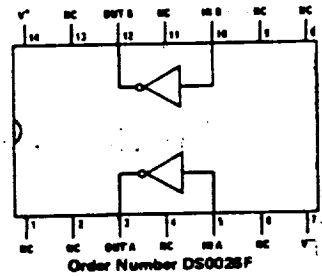
Order Number
DS0026CJ-8,
DS0026CN-8
or DS0026J-8
See NS Package J08A or N08A

TO-8 Package



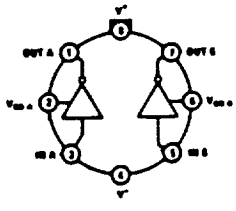
Order Number DS0026Q
or DS0026CG
See NS Package G12C

Flat Package



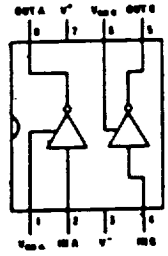
Order Number DS0026F
See NS Package F14A

TO-5 Package



Order Number DS0056H
or DS0056CH
See NS Package H08C

Dual-In-Line Package



Order Number
DS0056J-8, DS0056CJ-8
or DS0056CN-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

$V^+ - V^-$ Differential Voltage	22V	Operating Temperature Range	
Input Current	100 mA	DS0026, DS0056	−55°C to +125°C
Input Voltage ($V_{IN} - V^-$)	5.5V	DS0026C, DS0056C	0°C to +70°C
Peak Output Current	1.5A	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH} Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH} Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL} Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL} Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL} Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$			$V^-+0.7$	$V^-+1.0$	V
V_{OH} Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{BB} \geq V^+ + 1.0V$	DS0026	$V^+-1.0$	$V^+-0.7$		V
		DS0056	$V^+-0.3$	$V^+-0.1$		V
$I_{CC(ON)}$ "ON" Supply Current	$V^+ - V^- = 20V$ $V_{IN} - V^- = 2.4V$ (Note 6) (one side on)	DS0026		30	40	mA
		DS0056		12	30	mA
$I_{CC(OFF)}$ "OFF" Supply Current	$V^+ - V^- = 20V$,	70°C		10	100	μA
	$V_{IN} - V^- = 0V$	125°C		10	500	μA

Switching Characteristics ($T_A = 25°C$) (Notes 5 and 7)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON} Turn-on Delay	*(Figure 1)*		5	7.5	12	ns
	(Figure 2)			11		ns
t_{OFF} Turn-off Delay	*(Figure 1)*			12	15	ns
	(Figure 2)			13		ns
t_r Rise Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		15	18	ns
		$C_L = 1000$ pF		20	35	ns
	(Figure 2), (Note 5)	$C_L = 500$ pF		30	40	ns
		$C_L = 1000$ pF		36	50	ns
t_f Fall Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		12	16	ns
		$C_L = 1000$ pF		17	25	ns
	(Figure 2), (Note 5)	$C_L = 500$ pF		28	35	ns
		$C_L = 1000$ pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^-$ = 10V to 20V, C_L = 1000 pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

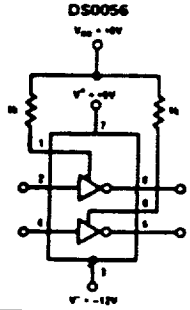
Note 4: All typical values for the T_A = 25°C.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1$ kΩ (for one side) when output is low.

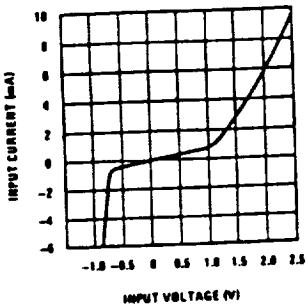
Note 7: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Typical V_{BB} Connection

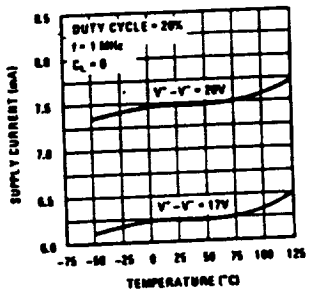


Typical Performance Characteristics

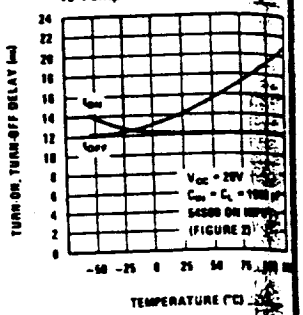
Input Current vs Input Voltage



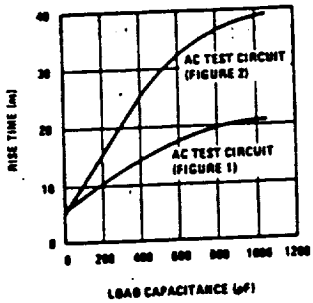
Supply Current vs Temperature



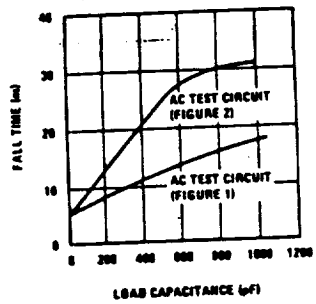
Turn-On and Turn-Off Delay vs Temperature



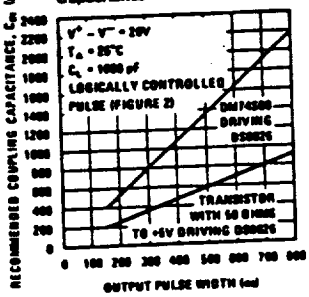
Rise Time vs Load Capacitance



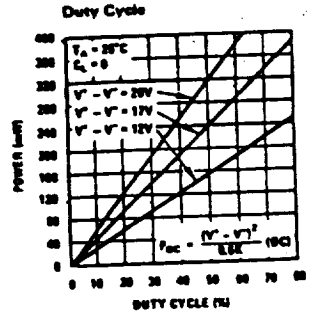
Fall Time vs Load Capacitance



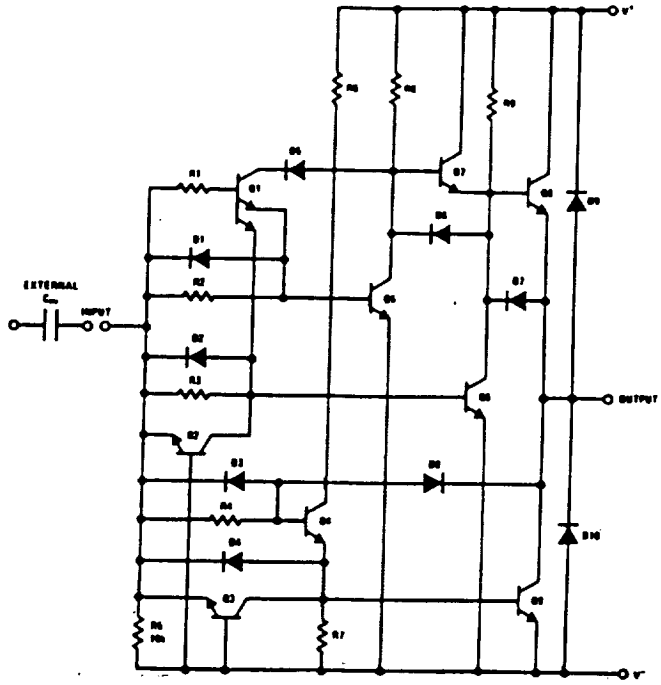
Recommended Input Coupling Capacitance



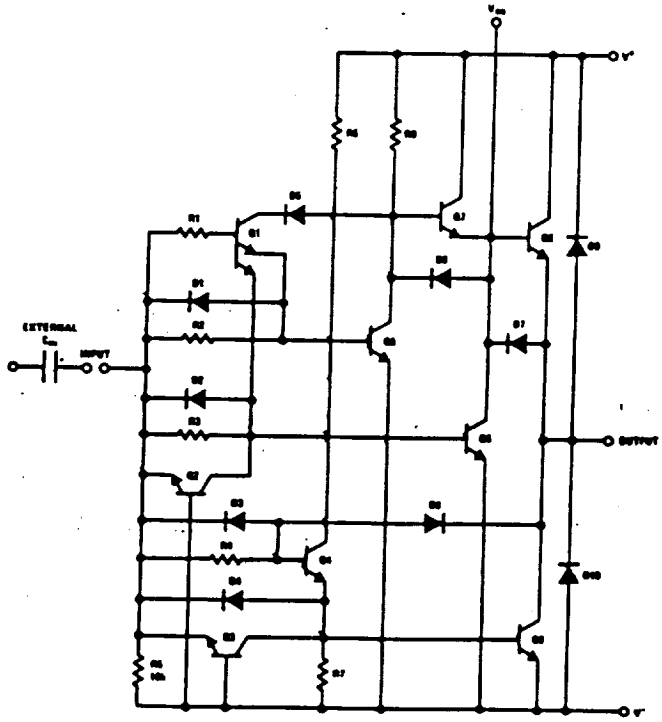
DC Power (P_{DC}) vs Duty Cycle



Schematic Diagrams



1/2 DS0026



1/2 DS0056

AC Test Circuits and Switching Time Waveforms

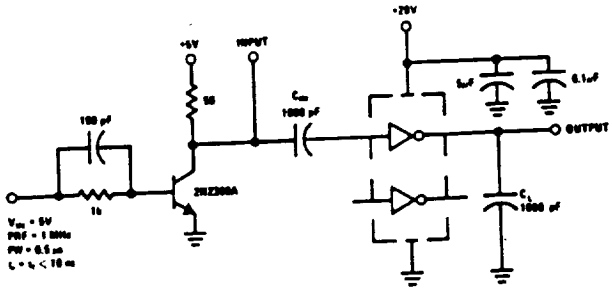


FIGURE 1.

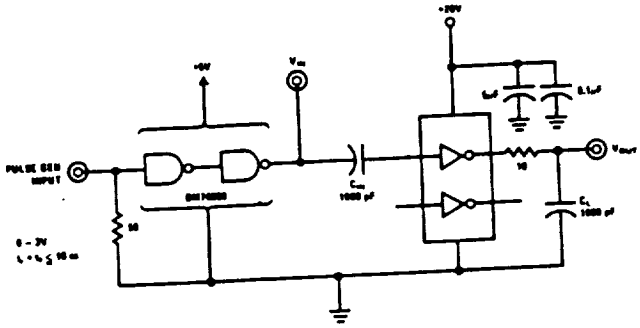
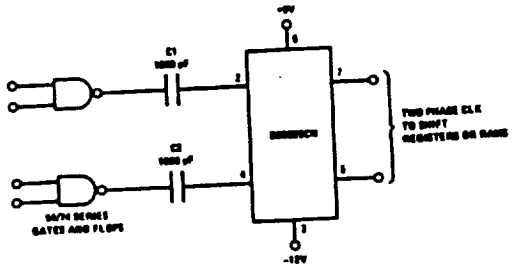


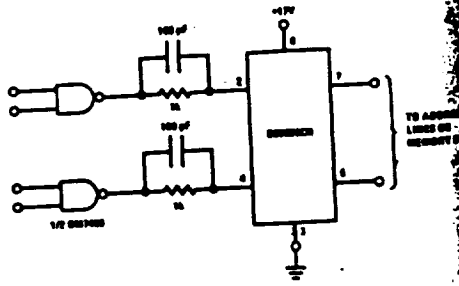
FIGURE 2.

Typical Applications

AC Coupled MOS Clock Driver



DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock

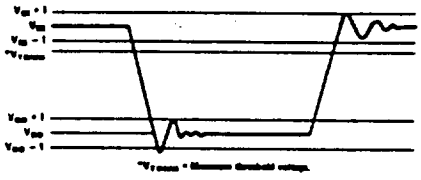


FIGURE 6. Clock Waveform

specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particulary difficult because of the relative magnitude of the allowable ringing, compared to the magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10 ohms to 20 ohms is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

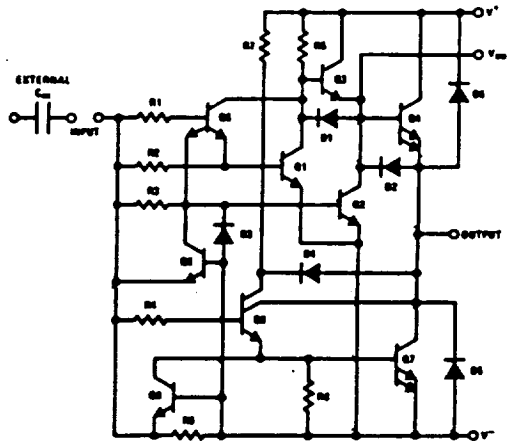


FIGURE 7. Schematic of 1/2 DS0056

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q4 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0V$ clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q4 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin or this line to zero.

Application Hints (Continued)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

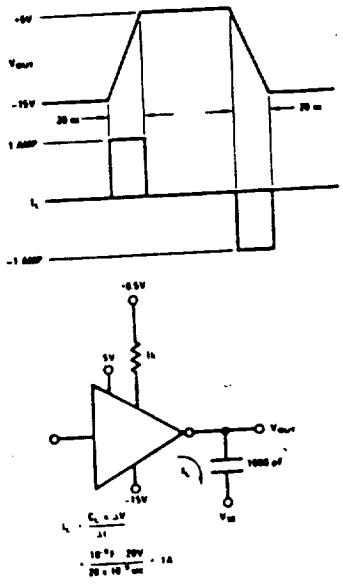


FIGURE 8. Clock Waveforms (Voltage and Current)

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since this noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock tranisent from the 7404 because of the inductance, L.

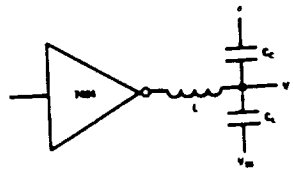


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\,mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

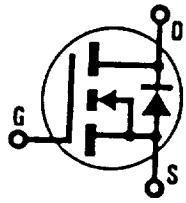
In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262 coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

Data Sheet No. PD-9.376C

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF840

N-CHANNEL POWER MOSFETs



IRF841

IRF842

IRF843

500 Volt, 0.85 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

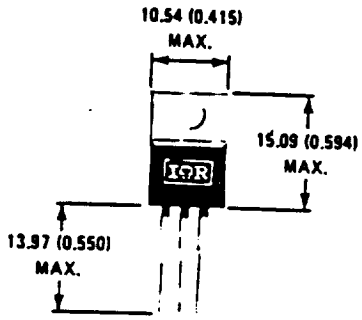
Features:

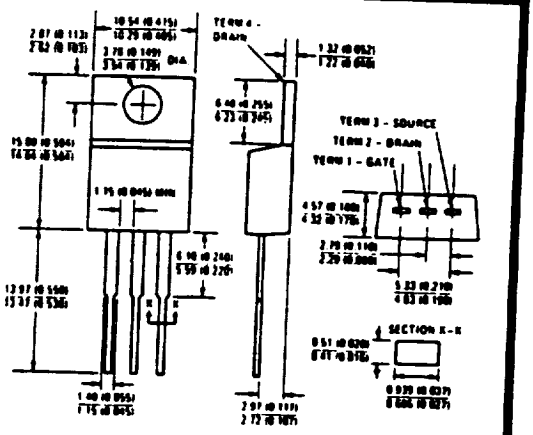
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF840	500V	0.85Ω	8.0A
IRF841	450V	0.85Ω	8.0A
IRF842	500V	1.10Ω	7.0A
IRF843	450V	1.10Ω	7.0A

CASE STYLE AND DIMENSIONS





Case Style TO-220AB
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

Parameter		IRF840	IRF841	IRF842	IRF843	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	32	32	28	28	A
		(See Fig. 15 and 16) L = 100μH				
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF840, IRF842	500	–	–	V	V_{GS} = 0V, I_D = 250μA
		IRF841, IRF843	450	–	–	V	
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF840, IRF841	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF842, IRF843	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF840, IRF841	–	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF842, IRF843	–	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	1225	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz, See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} = 200V, I_D = 4.0A, Z_o = 4.7Ω, See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	80	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	20	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF840 IRF841	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
		IRF842 IRF843	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF840 IRF841	–	–	32	A	
		IRF842 IRF843	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF840 IRF841	–	–	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 100A/μs
		IRF842 IRF843	–	–	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 100A/μs
t_{rr}	Reverse Recovery Time	ALL	–	1100	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.4	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

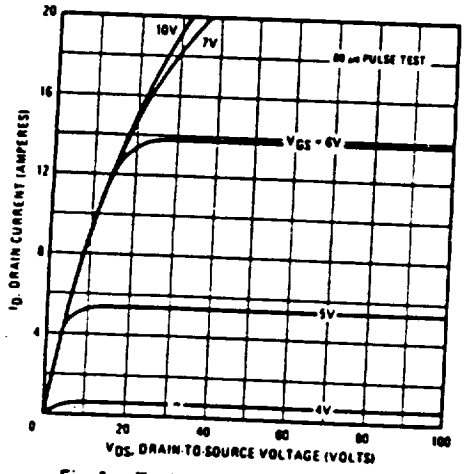


Fig. 1 — Typical Output Characteristics

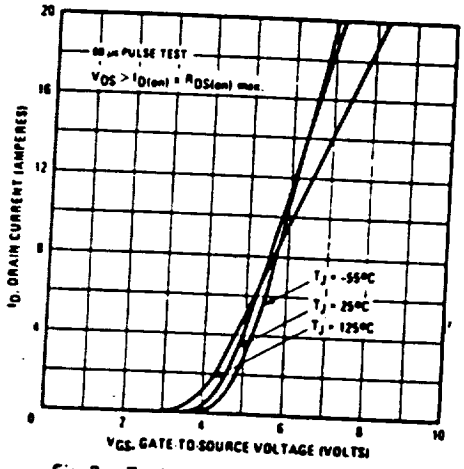


Fig. 2 — Typical Transfer Characteristics

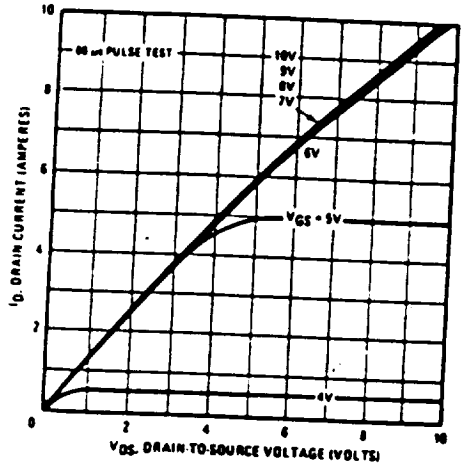


Fig. 3 — Typical Saturation Characteristics

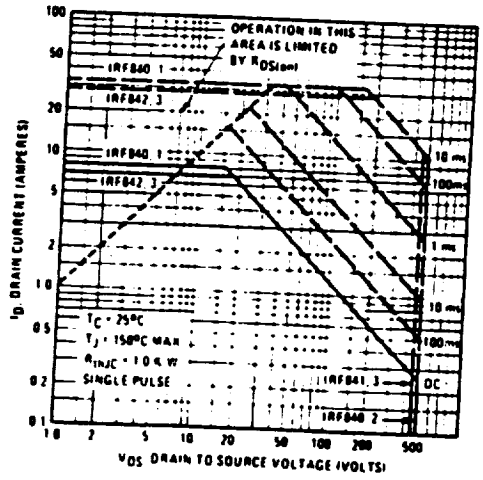


Fig. 4 — Maximum Safe Operating Area

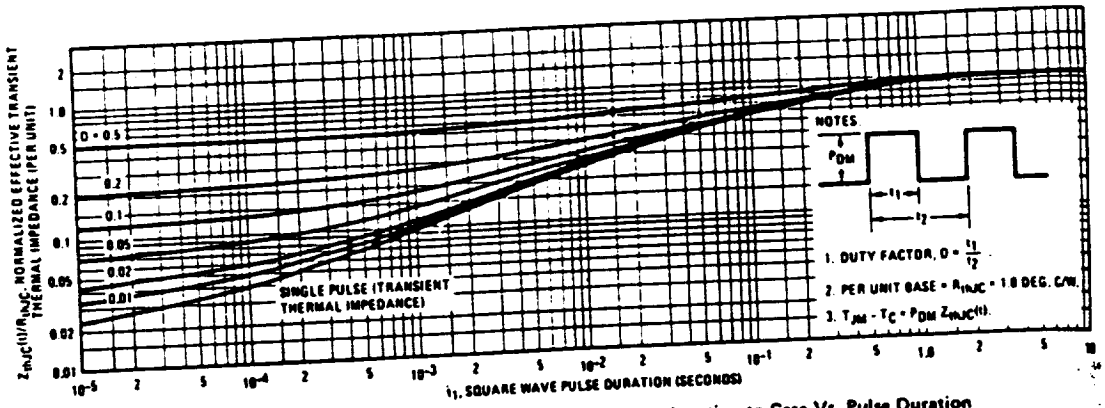


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

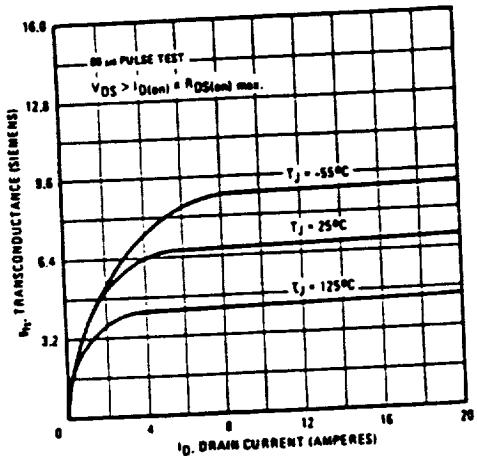


Fig. 6 – Typical Transconductance Vs. Drain Current

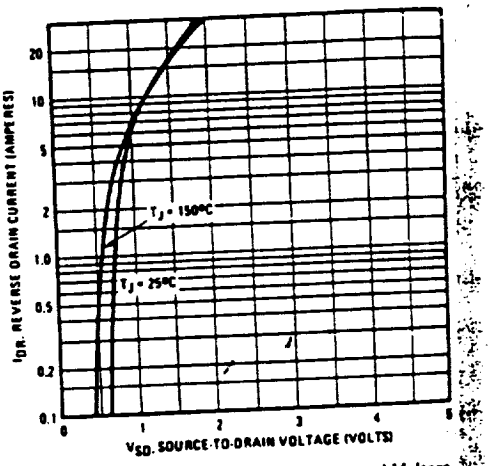


Fig. 7 – Typical Source-Drain Diode Forward Voltage

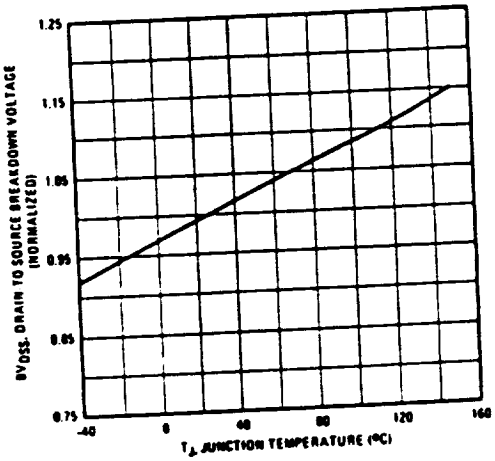


Fig. 8 – Breakdown Voltage Vs. Temperature

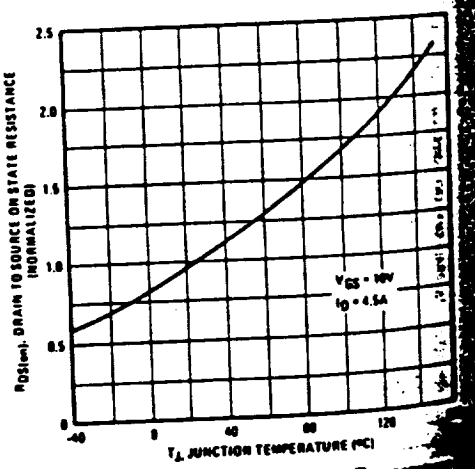


Fig. 9 – Normalized On-Resistance Vs. Temperature

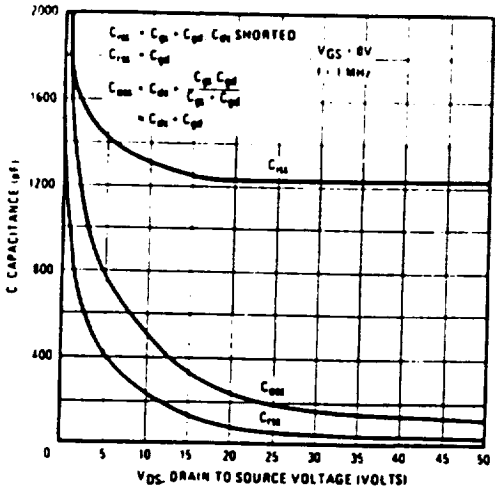


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

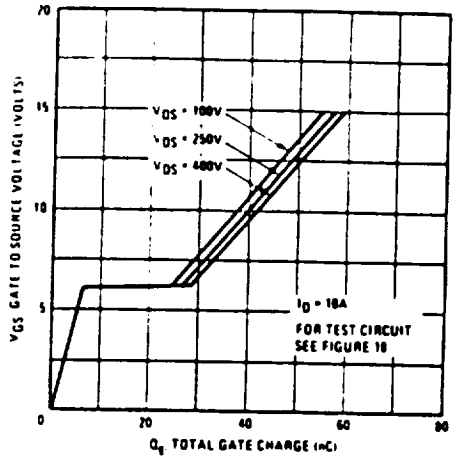


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

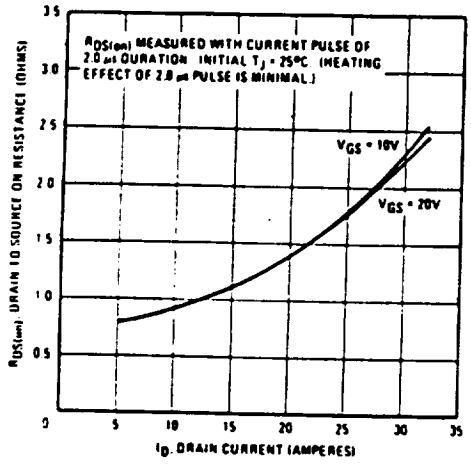


Fig. 12 – Typical On-Resistance Vs. Drain Current

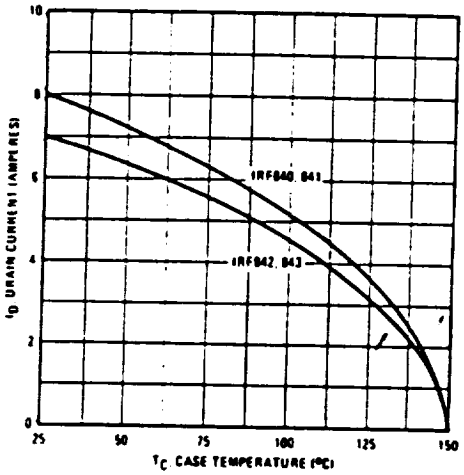


Fig. 13 – Maximum Drain Current Vs. Case Temperature

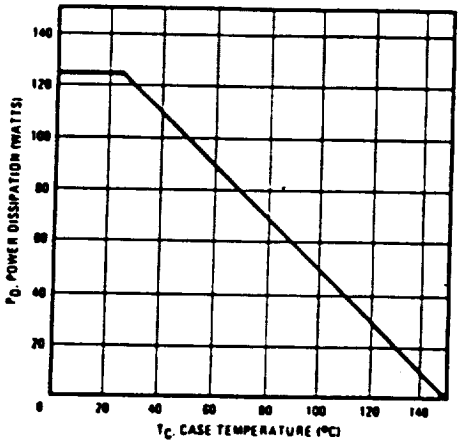


Fig. 14 – Power Vs. Temperature Derating Curve

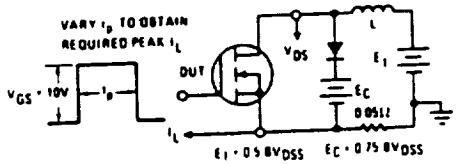


Fig. 15 – Clamped Inductive Test Circuit

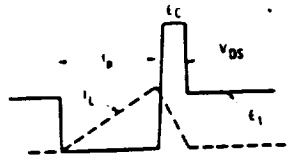


Fig. 16 – Clamped Inductive Waveforms

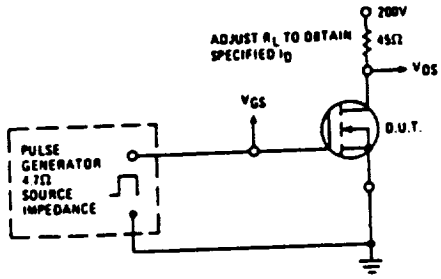


Fig. 17 – Switching Time Test Circuit

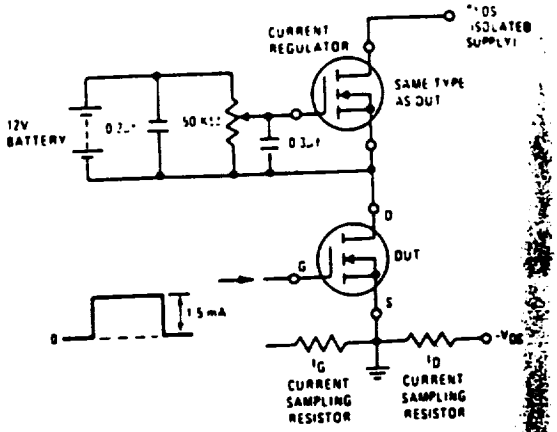


Fig. 18 – Gate Charge Test Circuit

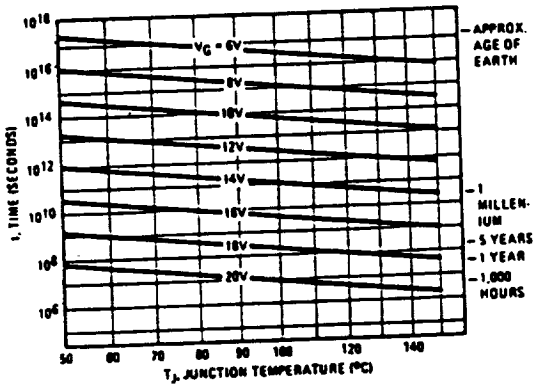


*Fig. 19 – Typical Time to Accumulated 1% Failure

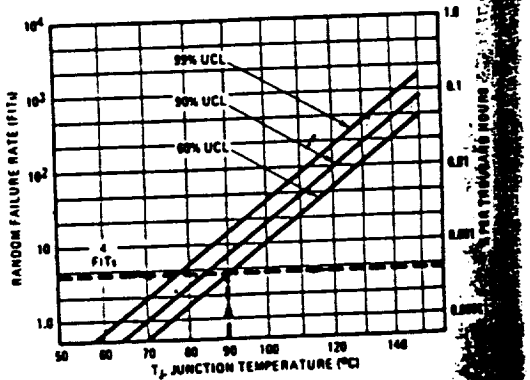


*Fig. 20 – Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1984. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.